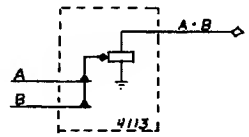
LOGIC DRAWINGS

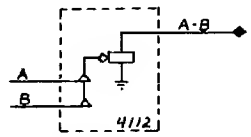
The symbology used in the LINC logic drawings is very similar to that used by Digital Equipment Corporation (DEC) of Maynard, Massachusetts. For a general explanation of this symbology, see DEC manual C-100. This manual also contains a description of each of the DEC logic packages used in the LINC. Other logic packages used in the LINC are described in volume 2 of the LINC Manufacturing Description.

DEC packages are identified by type numbers such as 4113, 4204, 4141, etc. Some of these packages can be jumpered internally to satisfy different loading conditions or to perform different logic functions. Packages used in the LINC indicate their jumpering configuration through suffixes appended to their type number. The package 4204, for example, appears as a plain 4204, a jumpered 4204A, and a jumpered 4204AC. The jumpering configuration specified by a suffix can be looked up in volume 2 of the LINC Manufacturing Description.

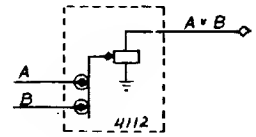
A broken line encloses each logic package or piece thereof that appears on a LINC logic drawing. The package type is written just inside the broken line, the packages frame location is written just outside. Minor variation from DEC symbology can always be resolved by looking up a particular package in the DEC manual and checking out the pins in questions. Grosser departures from DEC symbology are explained to the right.



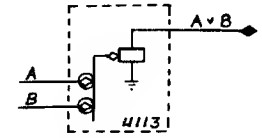
NEG. "AND"



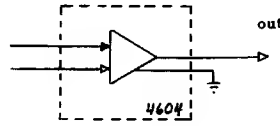
GND. "AND"



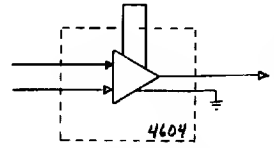
NEG. "OR"



GND. "OR"

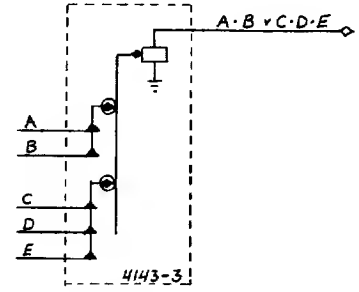


outpnt is a 0.4 nsec pulse.



jnmper makes ontput a 1.0 nsec pulse.

PULSE AMPLIFIERS



NEG. "AND-OR"

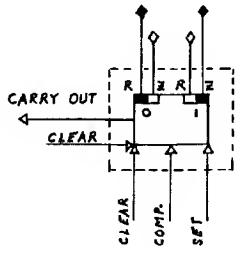
TIMING DIAGRAMS

Timing diagrams are used to show that occurence and relationship of the various operations involved in the execution of an instruction. In this notation, each of the principal flip-flop registers is represented by a horizontal line. Time is measured along the line from left to right, and operations involving the register are marked at their proper time of occurence. The registers R, L, and Z are shown only in those instructions that involve them. Registers B, C, P, S, and A are always shown. The operation of memory is indicated by a line marked "M." When this line is displaced upward, memory is in its read phase: when it's displaced downward, memory is in its write phase. A conditional operation of memory is indicated by a broken line.

Most operations occur at one of the standard event times marked along the top of the diagram by the numbers 0, 1, 2, and 3 (representing time pulses t_0, t_1, t_2, and t_3). Some operations, however, occur at other times. The clearing of S, for example, occurs at the end of the memory write gate if memory is operated. Otherwise it occurs at time t_2.

A vertical arrow indicates the modification of the contents of one register by the contents of another. The type of modification involved is specified to the right of the arrow head. All other operations are indicated by small vertical slash marks. If a slash mark indicates the clearing of a register, the register line will end at the slash mark. If the slash mark indicates anything else, the name of the operation is specified to its right.

Parentheses around the name of an operation indicate it as being conditional. Notes to one side of the diagram will specify the condition. Parentheses around the head of an arrow or around a slash mark indicate that more than one kind of operation can occur. Notes to the side of the diagram will call out the different operations possible and will specify the conditions under which they occur.



FLIP-FLOP

Outputs: 1. Output pins are shown twice, once for each side of the flip-flop. In this example, the output pins are R and Z. The example indicates that:

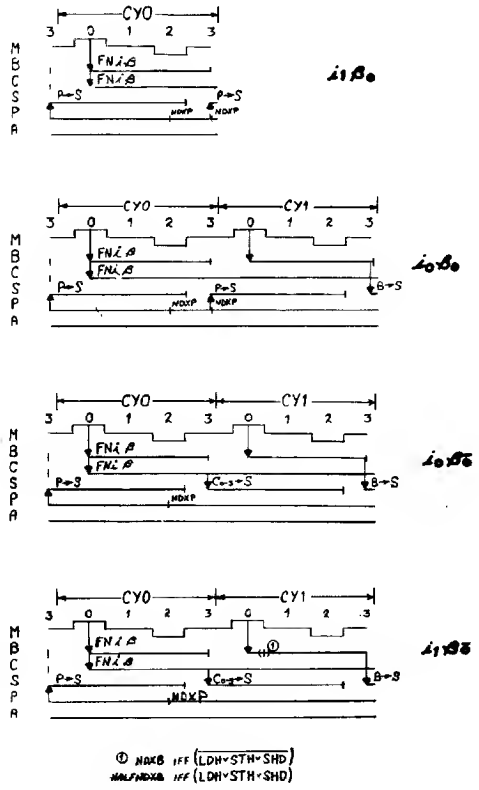
when the flip-flnp is a "zero," pin R is negative and pin Z is gnd.
when the flip-flop is a "one," pin Z is negative and pin R is gnd.

Inputs: 1. AC cnupled inputs are always drawn as though connected to a pnlse snnrce, even when the inpnt signal is not a pnlse.

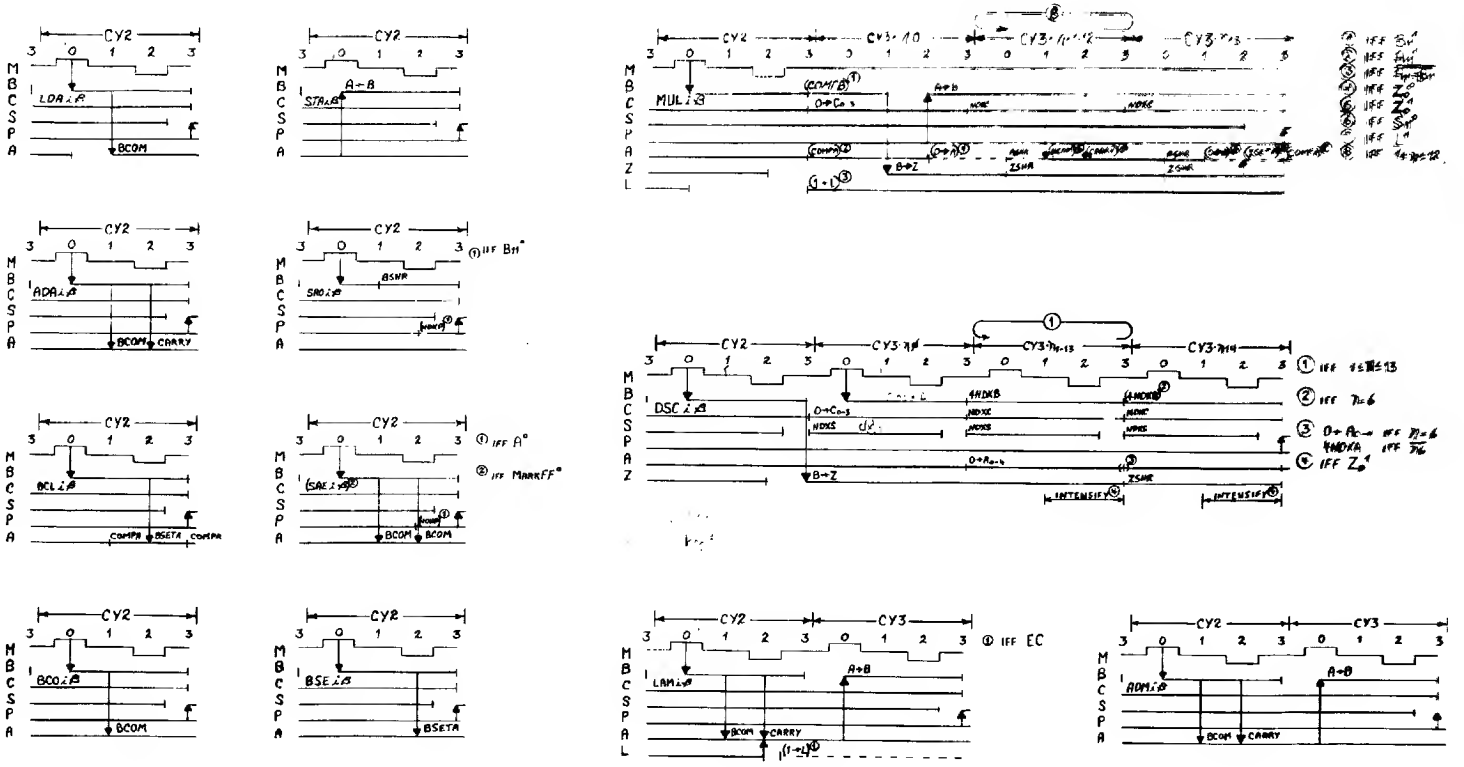
2. "Clear" inpnts may be drawn in either of the twn ways shown.

CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			SYMBOLOGY AND NOTATION
DWG.			
DATE	1000		CH.

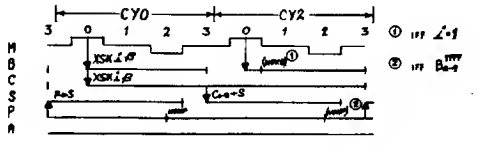
INDEX CLASS AND HALF WORD CLASS SET-UP CYCLES.

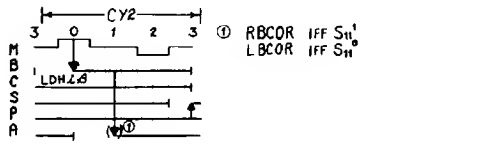


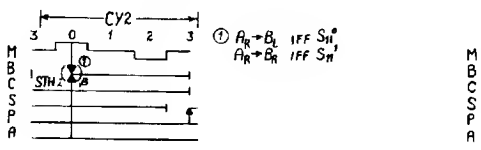
INDEX CLASS EXECUTION CYCLES.

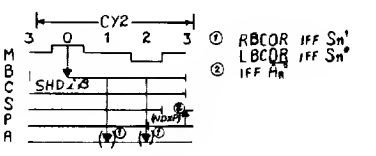


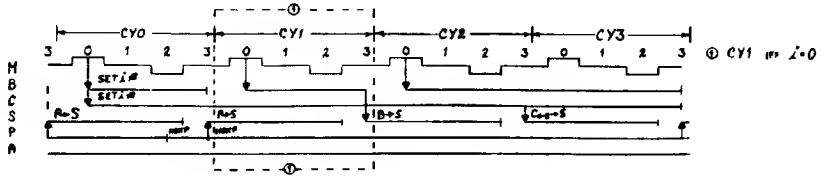
HALF WORD EXECUTION CYCLES.

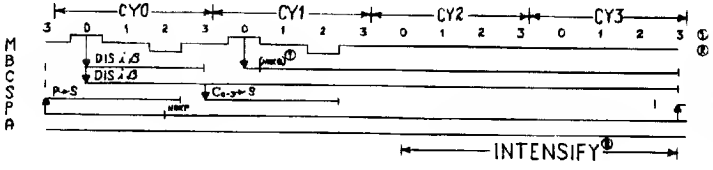






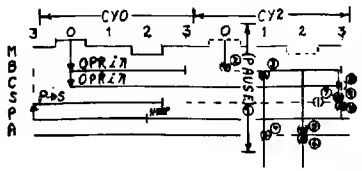






LINC — INSTRUCTION TIMING SHEET #1 — 1001

OPERATE CLASS INSTRUCTIONS.



① IFF i=1 AND $\overline{XCMET}$ RESUME WHEN $\overline{XCMET}$ OR QKRESTART)
② IFF MOUT
③ UN→B IFF UNEL
VN→B IFF VNEL
KB→B IFF 7115
RS→B IFF 7116
LS→B IFF 7117
④ O→A IFF (7115·7116·7117·CLEL ·SNEL·TNEL·BEGT)

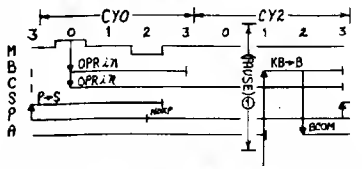
S

⑤ BCOM IFF $\overline{BEGT}$
⑥ SN→A IFF SNEL
TN→A IFF TNEL
⑦ O→A IFF GULP
NDXS IFF GULP·BEGT
⑧ O→C IFF GNIL
⑨ B→S IFF BEGT
⑩ P→S IFF GNIL

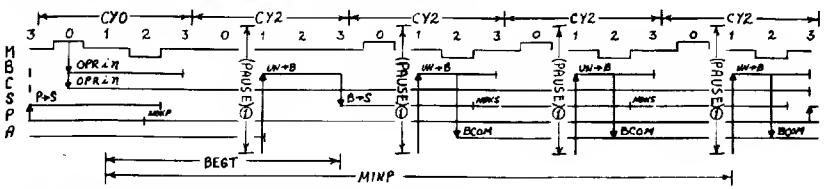
GULP = MINP ∨ MOUT ∨ BEGT

EXAMPLES OF OPERATE USAGE

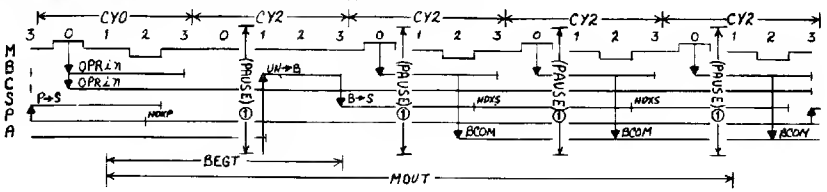
A. OPR i n15 (KBD)



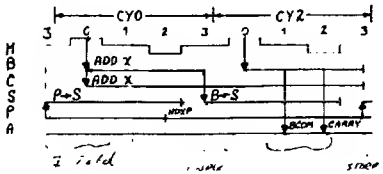
B. OPR • GULP (3 WORD TRANSFER INTO MEMORY)

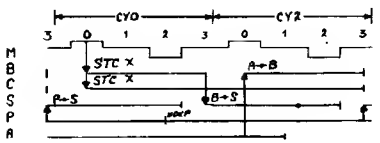


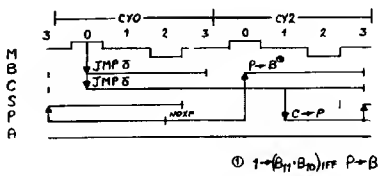
C. OPR • GULP (3 WORD TRANSFER OUT OF MEMORY)



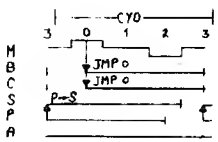
FULL ADDRESS INSTRUCTIONS.



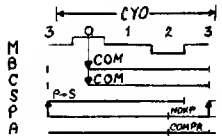


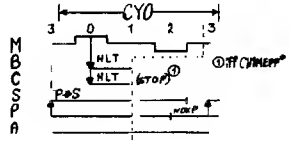


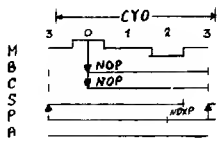
① $1 \rightarrow (B_{11} \cdot \overline{B_{10}})$ IFF P→B

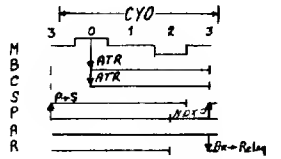


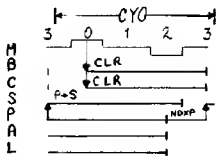
MISCELLANEOUS CLASS INSTRUCTIONS

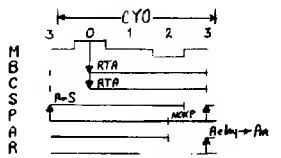




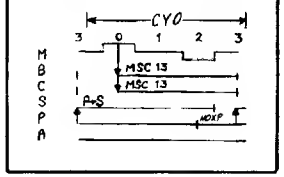


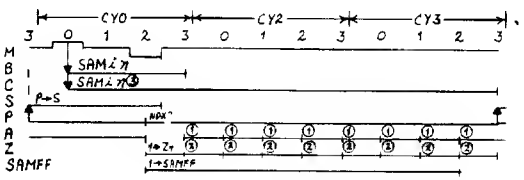


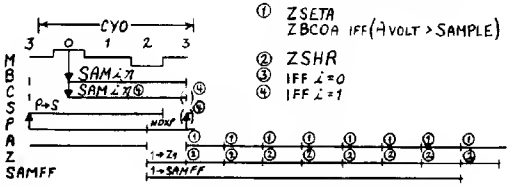




to be used with MARK program only



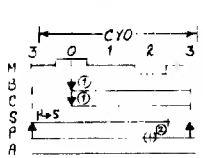




① ZSETA
ZBCOA IFF(AVOLT > SAMPLE)
② ZSHR
③ IFF i=0
④ IFF i=1

SKIP CLASS INSTRUCTIONS

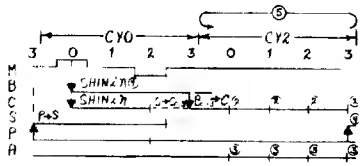
SKP i n_{0-5} = SNS i n_{0-5}
n_{10} = AZE i
n_{11} = APO i
n_{12} = IXE i
n_{13} = YBZ i
SXL i n_{0-14} = SXL i n_{0-14}
n_{15} = KST i



① SKP i n ∨ SXL i n
② NDXP IFF $\overline{CMET}$
ZNDXP IFF CMET

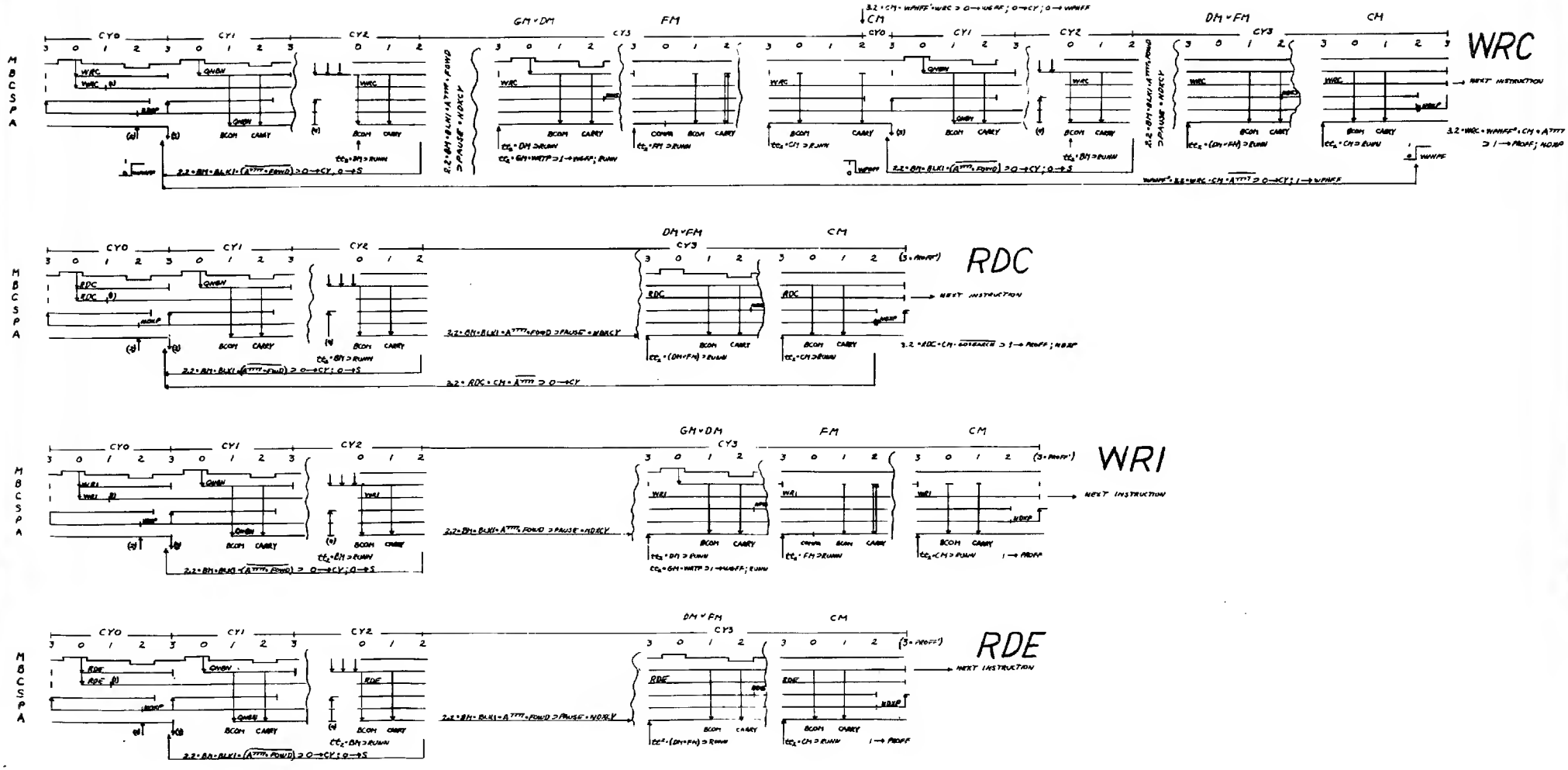
NOTE:
i_{0_1} Skip if condition met.
i_{1_1} Skip if condition not met.

ROTATE CLASS INSTRUCTIONS



① SHIN = POL∨ROR∨SCR
② NDXP IFF n=17
③ ASHR IFF ROR∨SCR
ASHL IFF ROL
④ P→S IFF n=17
⑤ IFF $\overline{n17}$

LINC		INSTRUCTION TIMING SHEET #2	
DATE	1002		DR



NOTES

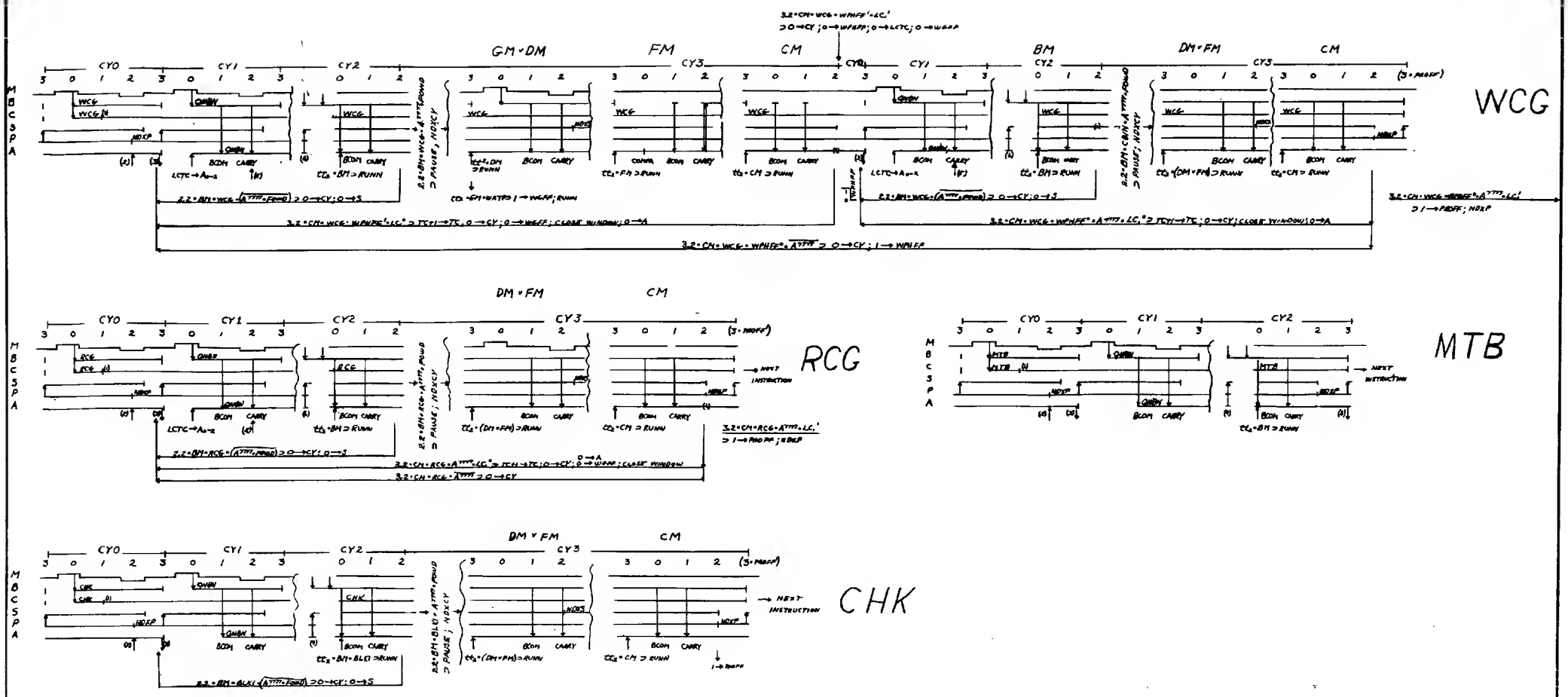
(1) SET UNIT

(2) $MQTM_L \rightarrow A_{n_L}$; $0 \rightarrow LCTC$; $1 \rightarrow WPMPF$; $0 \rightarrow PROFF$

(3) SET MOTION

(4) $FIXQ(0 \rightarrow A_{n-2})$; $A_{n-1} \rightarrow S_{n-1}$

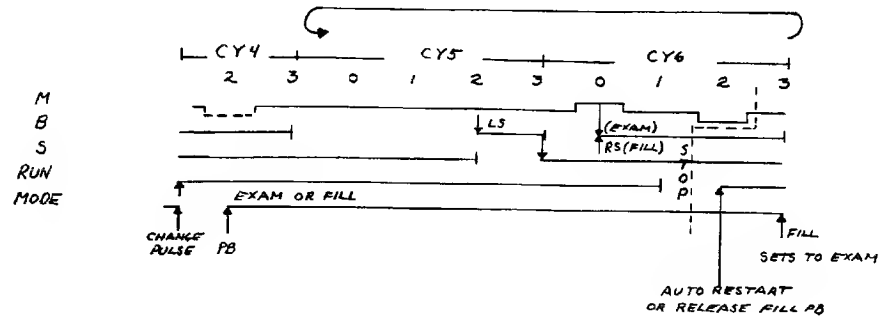
LINC	INSTRUCTION TIMING SHEET 3
	1003

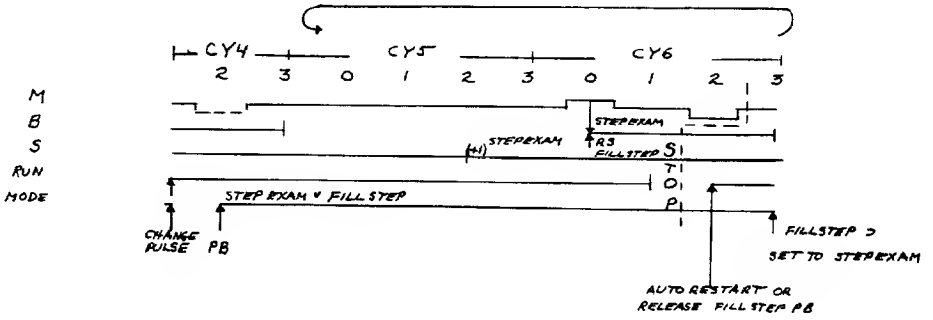


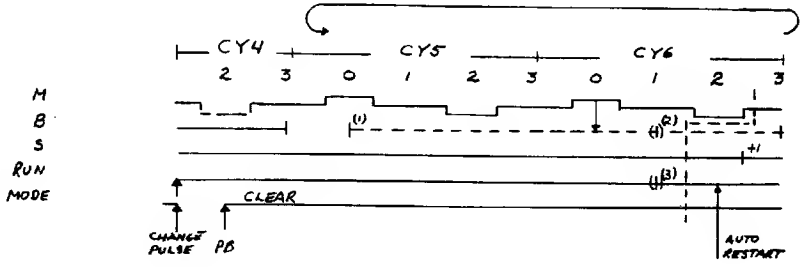
NOTES:

1. SET UNIT
2. $MOTN_n \rightarrow A_n$; 0 → LCTC ; 1 → WPHFF ; 0 → PROFF
3. SET MOTION
4. FIXQ ($0 \rightarrow A_{11-11}$) ; $A_{1-11} \rightarrow S_{3-10}$
5. $B_{-11} \equiv LCTC_{0-2} \geq 1 \rightarrow LC_1$
6. FIXQR($0 \rightarrow A_{2-8}$) ; $A_{0-2} \rightarrow S_{8-10}$

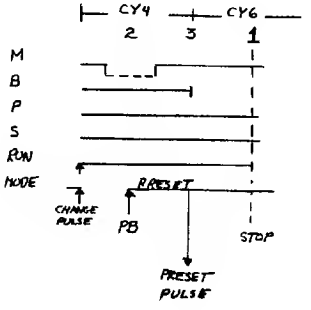
LINC		INSTRUCTION TIMING	
		SHEET 4	
DATE	1004	CR	

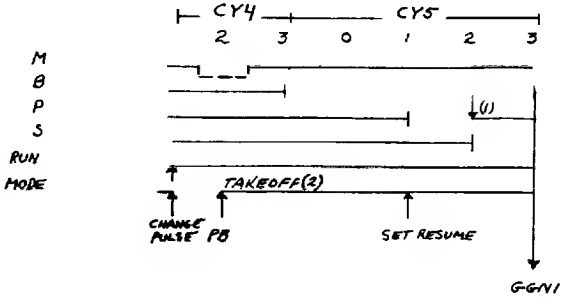






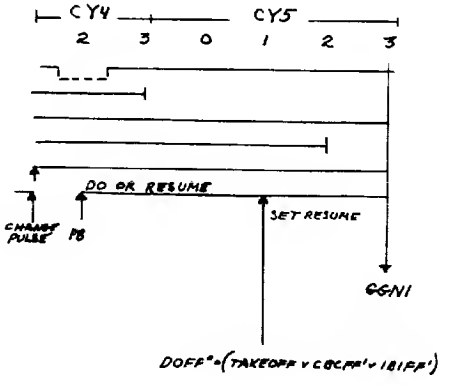
(1) $S_{11}' \supset$ SET B
(2) $S_{11}' \cdot \overline{B^0} \supset$ COMPB
(3) $\overline{B^0} \cdot (S_{10}^* \vee MET11) \supset$ STOP





(1) START 20 ⊃ 20 → P
" 400 ⊃ 400 → P
" RS ⊃ RS → P
MARK ⊃ 40 → P

(2) TAKEOFF = ST20FF' ∨
ST400FF' ∨ STRSFF' ∨ MARKFF'



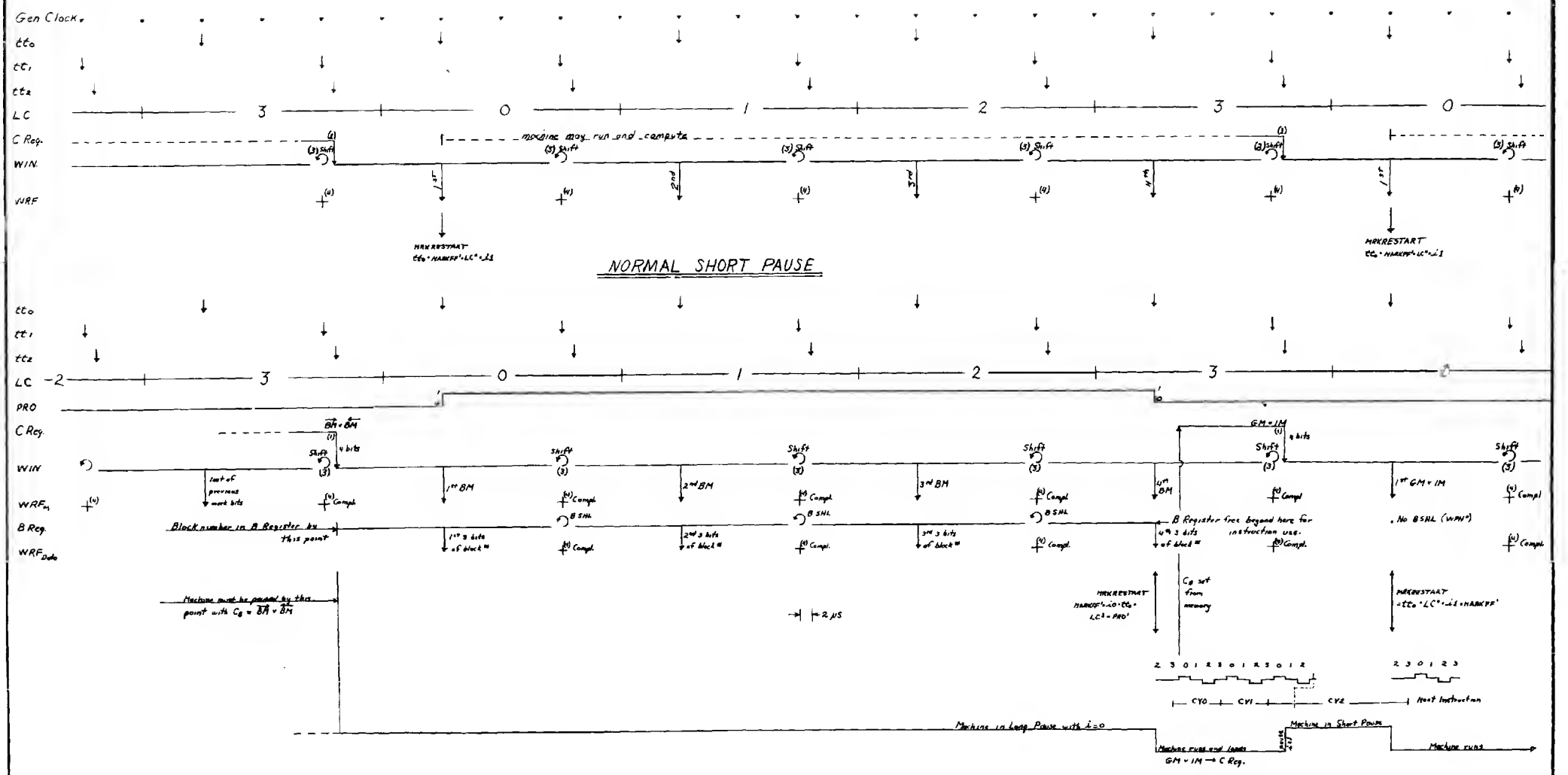
REVISION LETTER	APP'D BY	DATE	CHANGES

LINC

CONSOLE FUNCTION TIMING DIAGRAM

ENG.

DATE 1005 CH. E



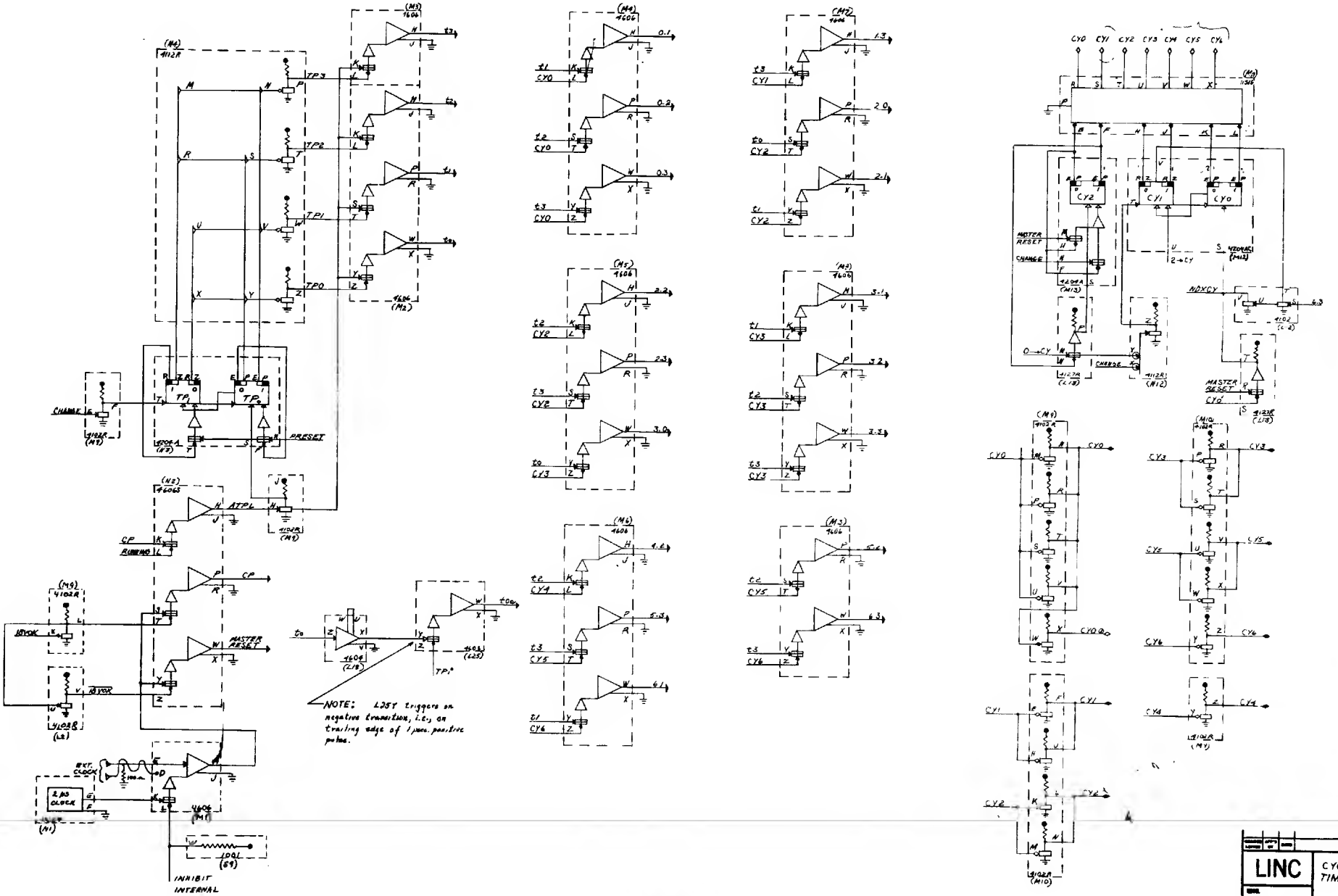
Notes:
(1) Machine must be paused by this time with next mark in $C_0 \cdot tt_2 \cdot LC^3$ jams $C_8 \rightarrow WIN$

(2) Shift next bit for mark track into leftmost bit of word (WIN_2). Shift in zeros from right so cleared before load from C_{MQ}

(4) Complement WRF_M of tt_1 time; tt_0's load is from WIN_3.

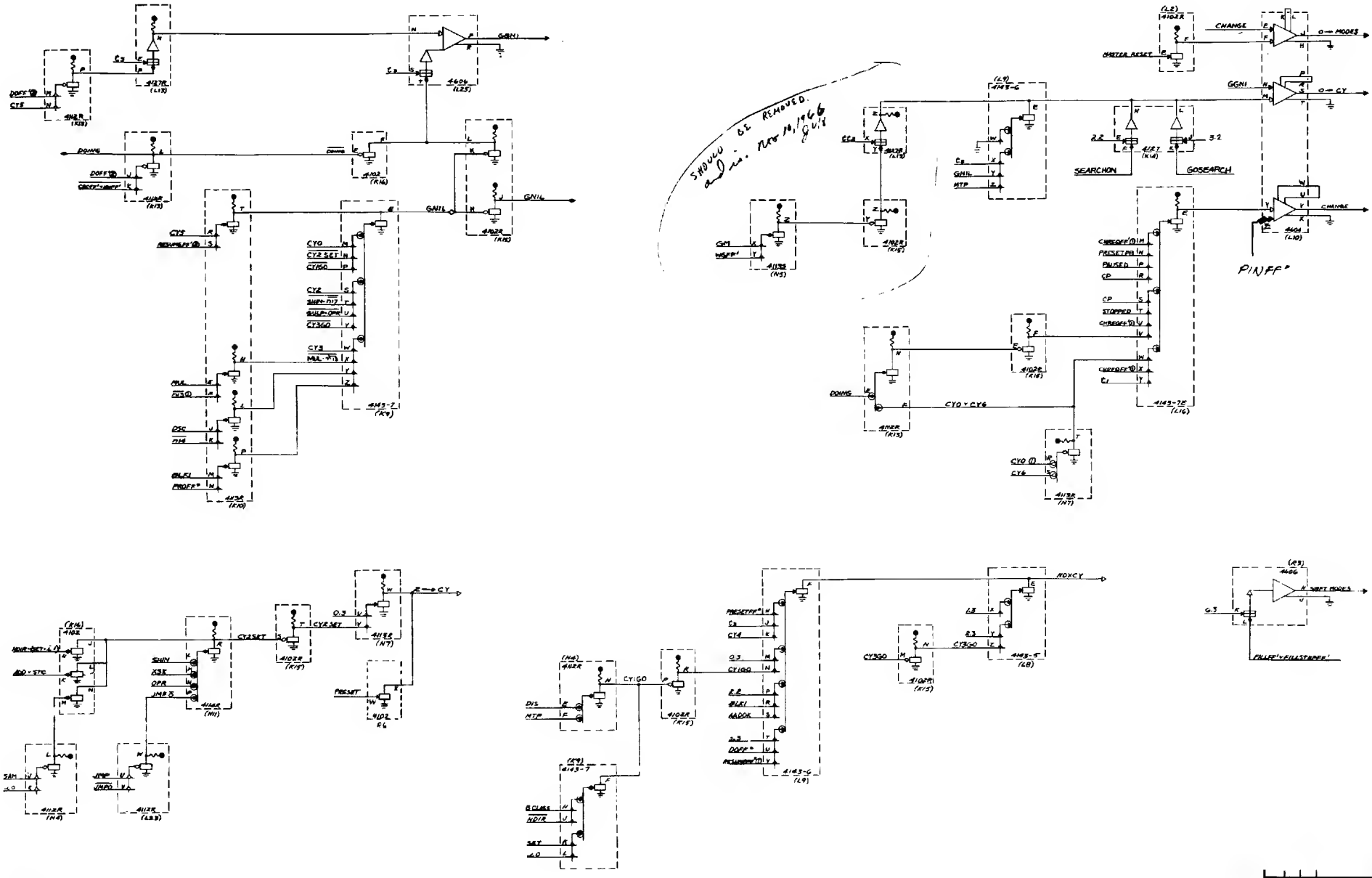
LINC	TAPE MARKING TIMING DIAGRAM	
	1006	

1008	D → CY
1003	A → CY
EXT.	IBYOK +
1005	CHANGE
EXT.	EXT. CLOCK
EXT.	INHIBIT INT. CLOCK
1002	NDXCY
1018	PRESET
1009	RUNNING



LINC | CYCLES AND TIME PULSES | DATE 1007

1007	$t_0 - t_3$
1033	$t_{10} - t_{12}$
1034	WGFF



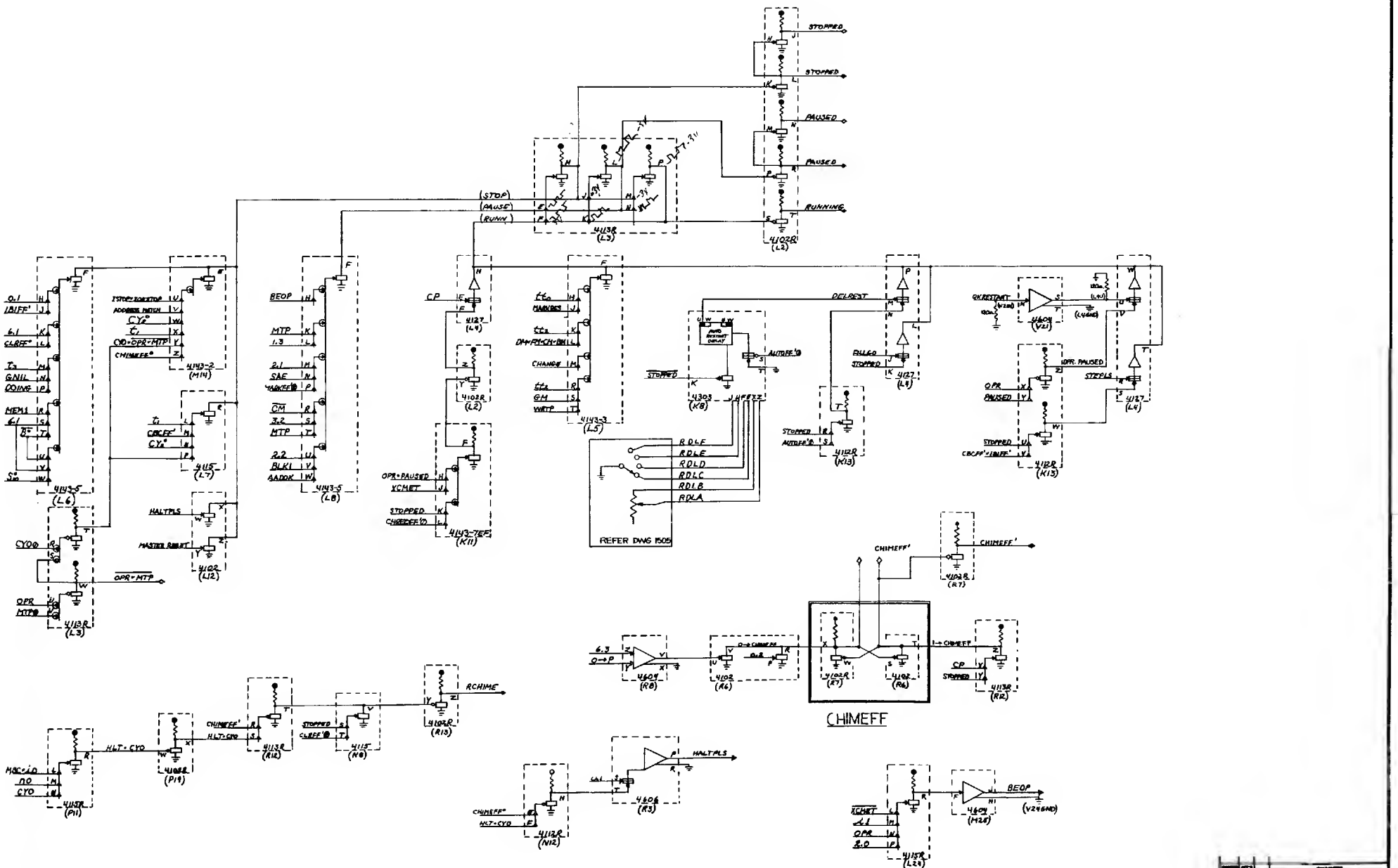
LINC	MODE AND CYCLE CONTROL LOGIC
DATE	1008

1007	0.0 – 6.3
1017	0 → P
1036	AADOK
1031	ADDRESS MATCH
1018	AUTOFF
1016	B°
1026	BLKI
1018	CBCFF
1018	CBCFF' ∨ IBIFF'
1005	CHANGF
1018	CHREQFF
1018	CLRFF

1026	CM Φ
1007	CP
1007	$CY_0 - CY_5$
1007	CY0 – CY6
1026	DM ∨ FM ∨ CM ∨ BM
1005	DOING
1018	FILLGO
1024	GM
1005	GNIL
1018	IBIFF
1012	INSTRUCTIONS Φ
1020	INSTRUCTIONS Φ

1018	ISTOP ∨ XOESTOP
1018	MARKFF
1026	MARKRES
1007	MASTER RESET
1030	MEM1
1020	MSC – 10
EXT.	QKRESTART
EXT.	RDLA – RDLF
1013	$S_0 - S_{11}$
1018	STEP13
1007	$t_0 - t_3$
1023	$tt_0 - tt_{12}$

1021 | XCMET



LINC

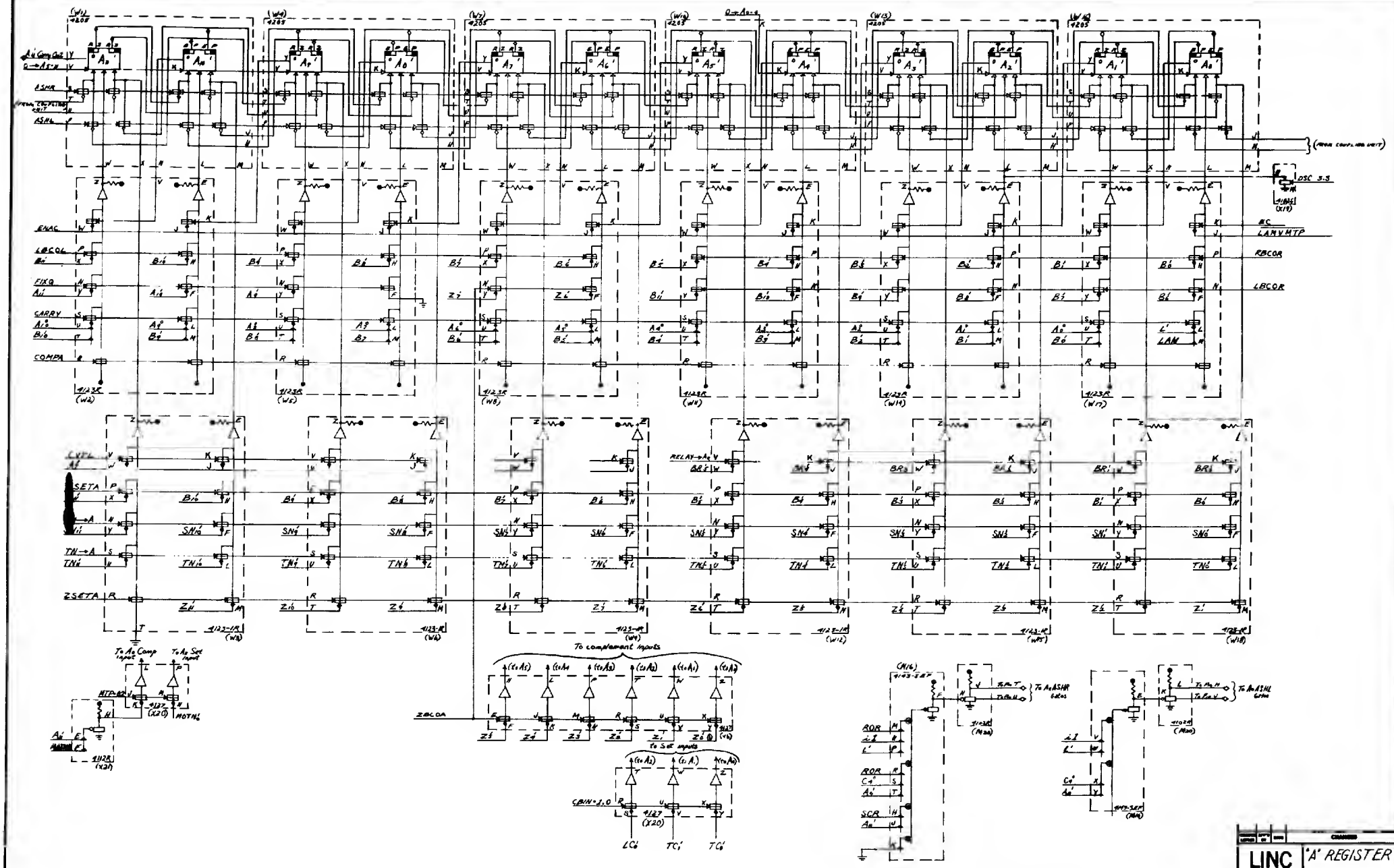
RUN – PAUSE – STOP LOGIC

DATE 1009

1015	$0 \rightarrow A_{0-4}$
1015	$0 \Rightarrow A_{0-11}$
1015	ASHL
1015	ASHR
1011	$B_0 - B_{11}$
1033	$BR_0 - BR_{11}$
1015	BSETA
1012	$C_0 - C_{11}$
1015	CARRY
1036	CBIN - 1.0
1015	COMPA
1037	CVPL

1036	DSC - 3.3
1014	EC
1015	ENAC
1015	FIXQ
1012	iO - i1
1030	INSTRUCTIONS
1014	L
1030	LAM + MTP
1015	LBCOL
1015	LBCOR
1033	$LC_0 - LC_1$
1036	$MSTM_0 - MSTM_1$

1015	RBCOR
1015	RELAY $\rightarrow A_R$
1015	SN $\rightarrow$ A
EXT.	$SN_0 - SN_{11}$
1033	$TC_0 - TC_1$
1015	TN $\rightarrow$ A
EXT.	$TN_0 - TN_{11}$
1014	$Z_0 - Z_{11}$
1037	ZBCOA
1015	ZSETA



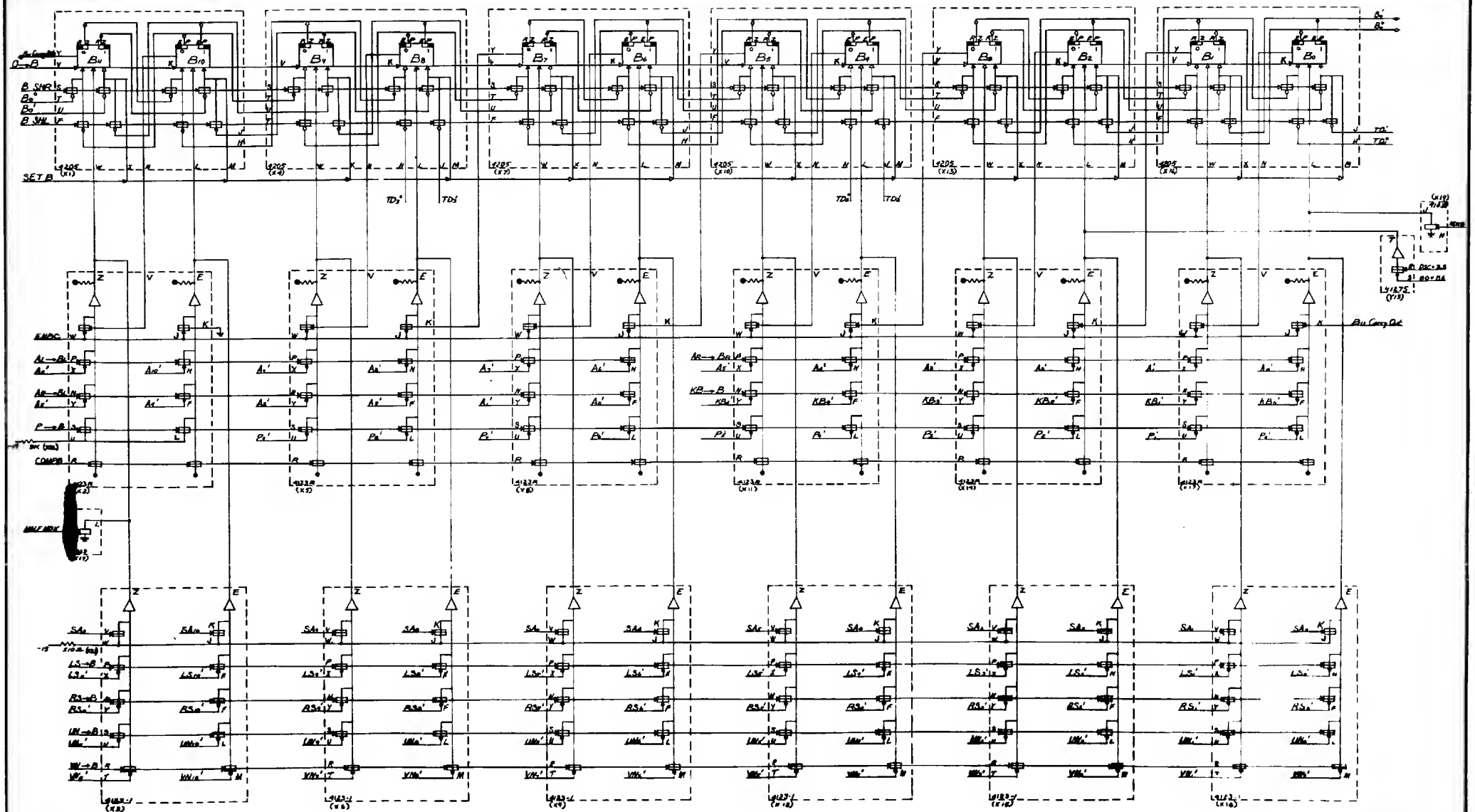
LINC "A" REGISTER

DATE 1010

1016	$0 \rightarrow B$
1016	$A_0 - A_5$
1016	$A_6 \rightarrow B_6$
1016	$A_{7,8} \rightarrow B_{7,8}$
1016	BSNL
1016	BSNR
1016	COMPB
1030	DSC·3.3
1016	EMBC
1016	HALFMDX
1016	$LS \rightarrow B$
EXT.	$LS_0 - LS_4$

1015	$MQ \rightarrow MB$
1016	MDXB
1016	$P \rightarrow B$
1013	$P_0 - P_8$
1016	$RS \rightarrow B$
EXT.	$RS_0 - RS_4$
1032	$SA_0 - SA_4$
1016	SETB
1024	$TD_1 - TD_3$
1016	$UN \rightarrow B$
EXT.	$UN_0 - UN_4$
1016	$VN \rightarrow B$

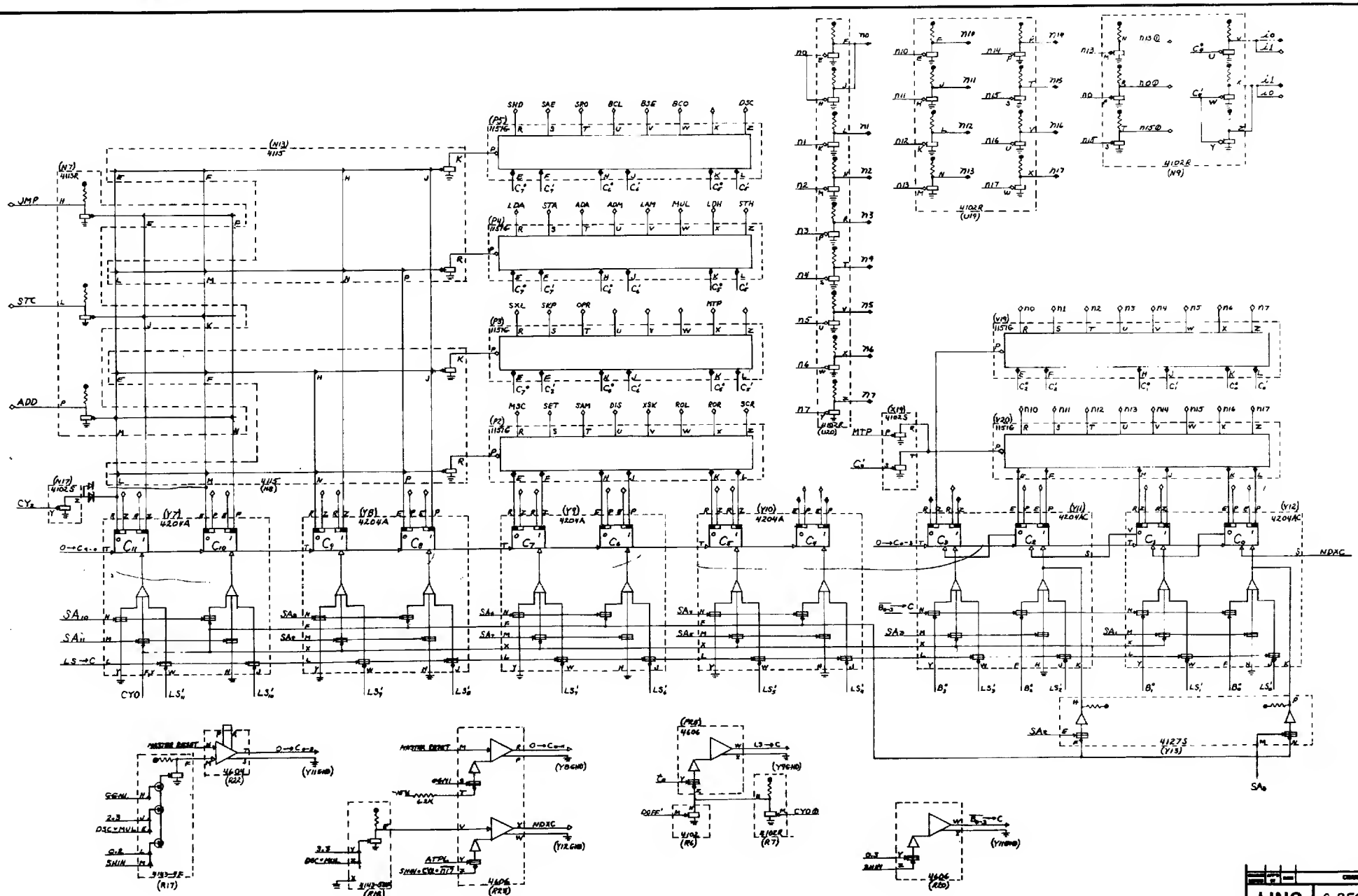
EXT. | $VN_0 - VN_4$



LINC | B REGISTER | 1011

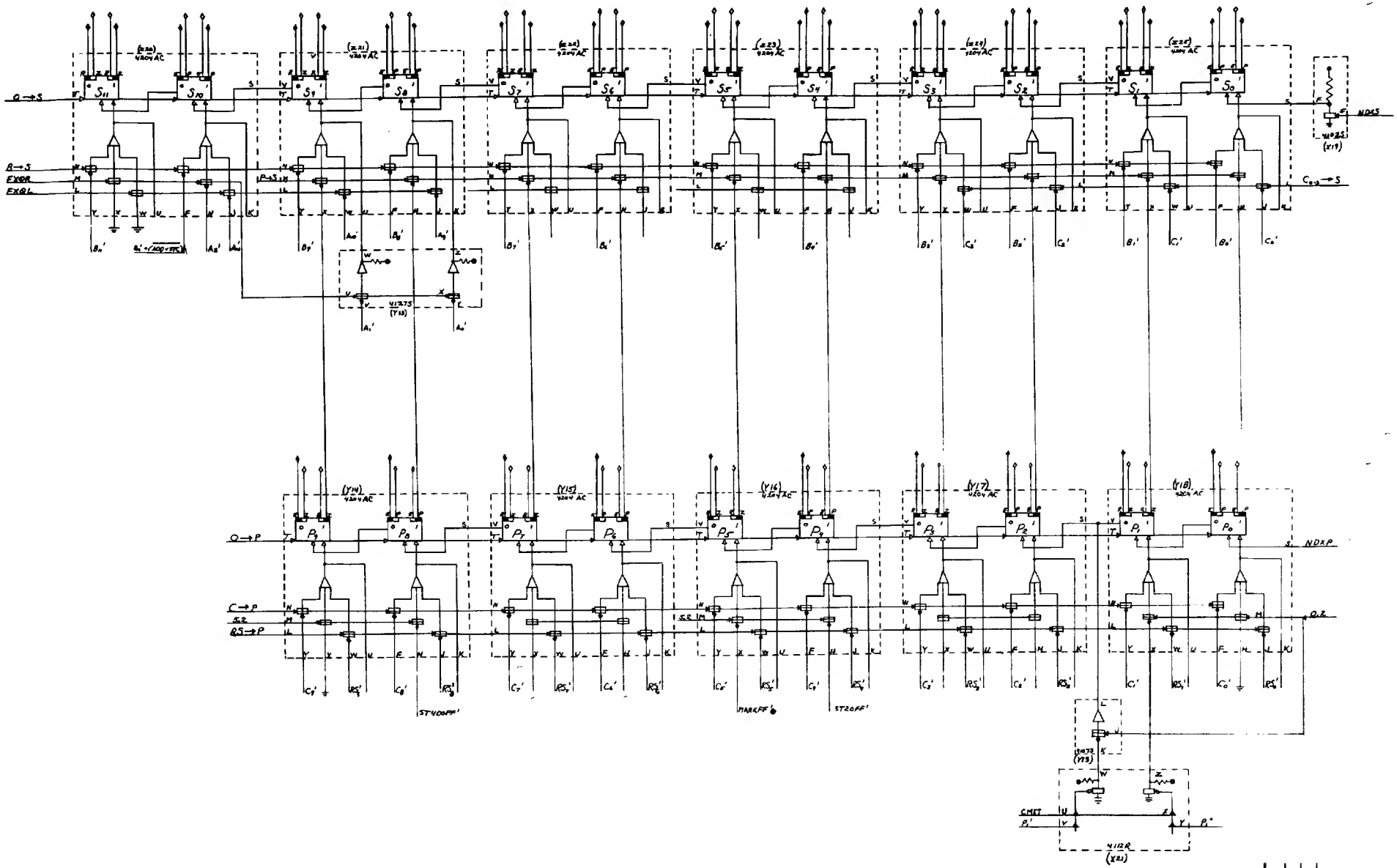
1007	0.0 – 6.3
1007	ATPL
1007	$CY_0 - CY_2$
1007	CY0 – CY6
1018	DOFF
1020	DSC + MUL
1008	GGNI
1020	INSTRUCTIONS +
EXT.	$LS_0 - LS_{11}$
1007	MASTER RESET
1028	$SA_0 - SA_{11}$
1020	SHIN

1015 | $SHIN \cdot CY2 \cdot \overline{R17}$



1007	0.0 – 6.3
1017	0 → P
1017	0 → S
1010	$A_0 - A_8$
1017	B → S
1011	$B_0 - B_8$
1030	$B_0' \cdot (ADD\ ETC.)$
1017	C → P
1017	$C_{0-8} \rightarrow S$
1012	$C_0 - C_8$
1017	CMET
1017	FXQL

1017	FXQR
1018	MARKFF
1017	NDXP
1017	NDXS
1017	P → S
1017	RS → P
EXT.	$RS_0 - RS_{11}$
1018	ST20FF
1018	ST400FF



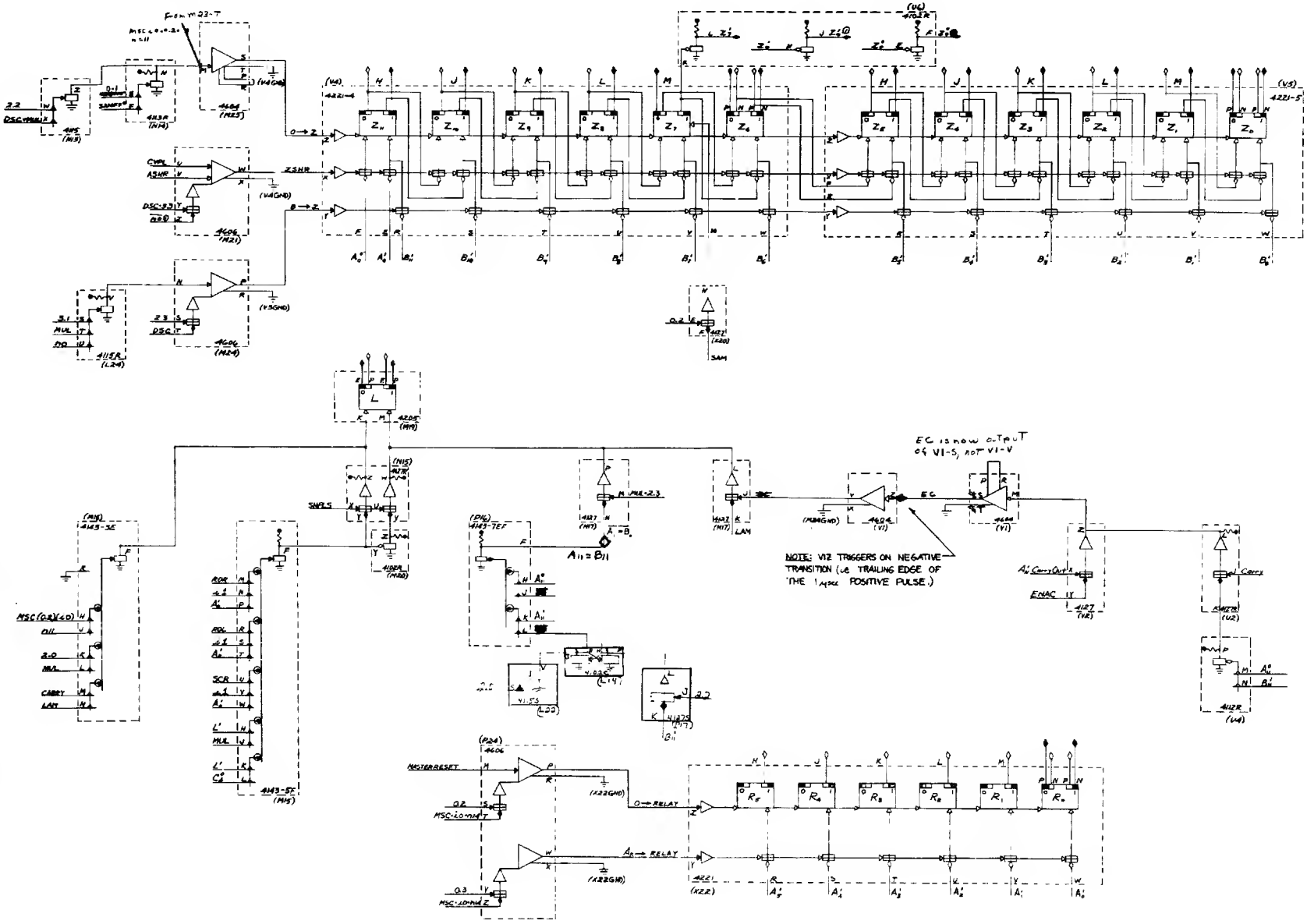
LINC

P & S REGISTERS

1013

1007	0.0 – 4.3
1010	$A_0 - A_{11}$
1015	ASHR
1011	$B_0 - B_{11}$
1012	$C_0 - C_{11}$
1015	CARRY
1027	CYPL
1020	DSC · 3.3
1020	DSC · MUL
1015	ENAC
1028	GGN1
1012	L0 – L1

1030	INSTRUCTIONS
1007	MASTER RESET
1030	MSC · L0 · nM
1020	MSC · L0 · 0.2
1030	MUL · 2.3
1012	n0 – n17
1027	SAMFF
1015	SHPLS
1015	MSC · L0 · 0.2 · M = 11



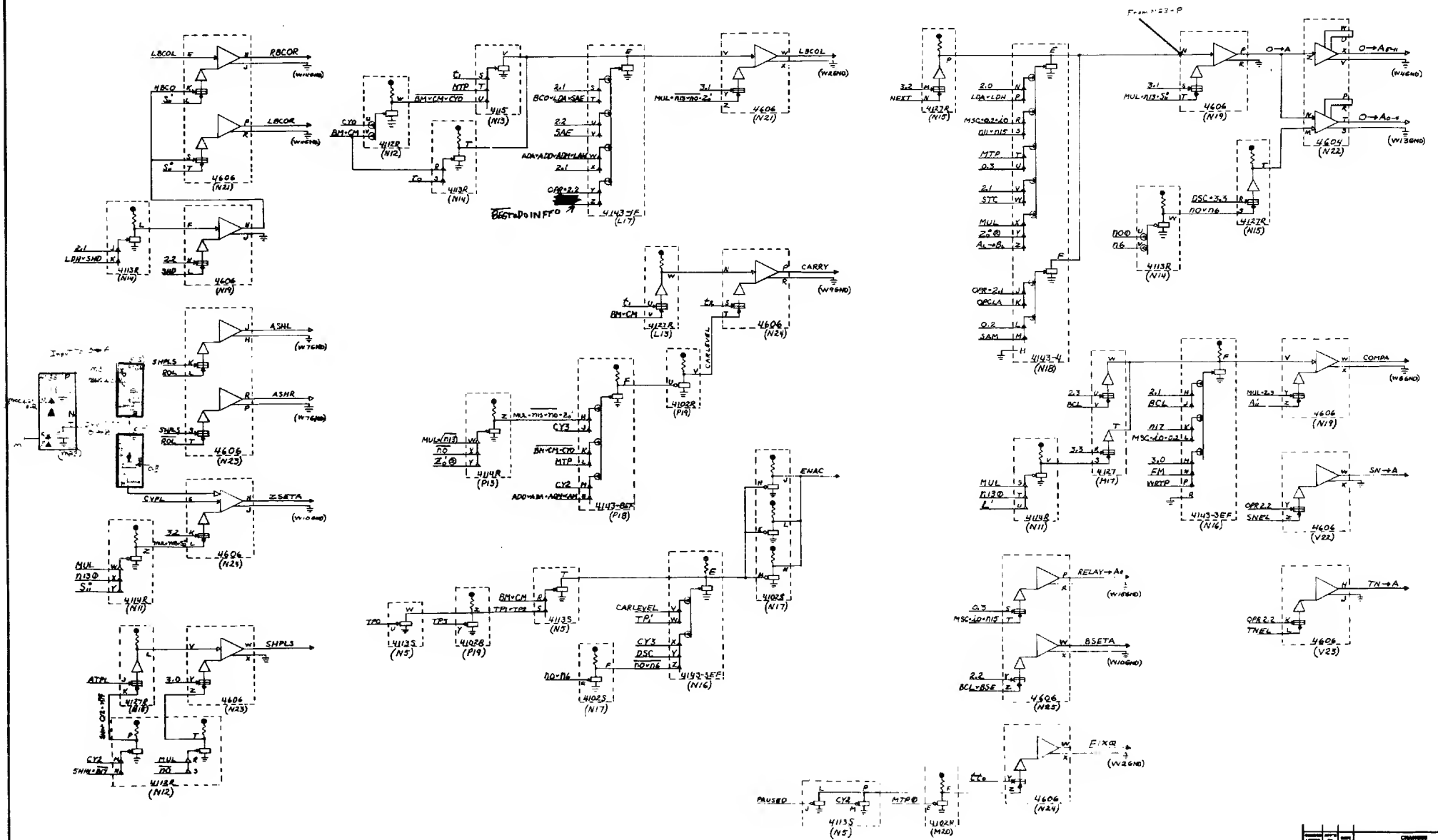
LINC		CHANGE	
			L, Z → R REGISTERS
DATE	1014	SHT	

1007	0.0 – 6.3
1010	$A_0 - A_{11}$
1016	$A_L \rightarrow B_L$
1020	ADD ∨ ADA ∨ ADM ∨ LAM
1007	ATPL
1020	BCL ∨ BSE
1020	BCO ∨ LDA ∨ SAE
1020	BF6T ◆
1026	BM ∨ CM
1027	CVPL
1007	CY0 – CY6
1020	DSC · 3.3

1024	FM
1012	INSTRUCTIONS ◇
1020	INSTRUCTIONS ◆
1014	L
1020	LDA ∨ LDH
1020	LDH ∨ SHD
1020	MSC · 10 · n15
1020	MSC · 10 · 0.2
1020	MUL · 2.3
1008	MUL · $\overline{n13}$
1015	MUL · n13 · S_{11}°
1012	n0 – n17

1020	n11 ∨ n15
1026	NEAT
1020	OPCLA
1020	OPR · 2.1
1020	OPR · 2.2
1009	PAUSED
1013	$S_0 - S_{11}$
1020	SHIN · $\overline{n17}$
EXT.	SNEL
1007	$t_0 - t_3$
1023	$tt_0 - tt_2$
EXT.	TNEL

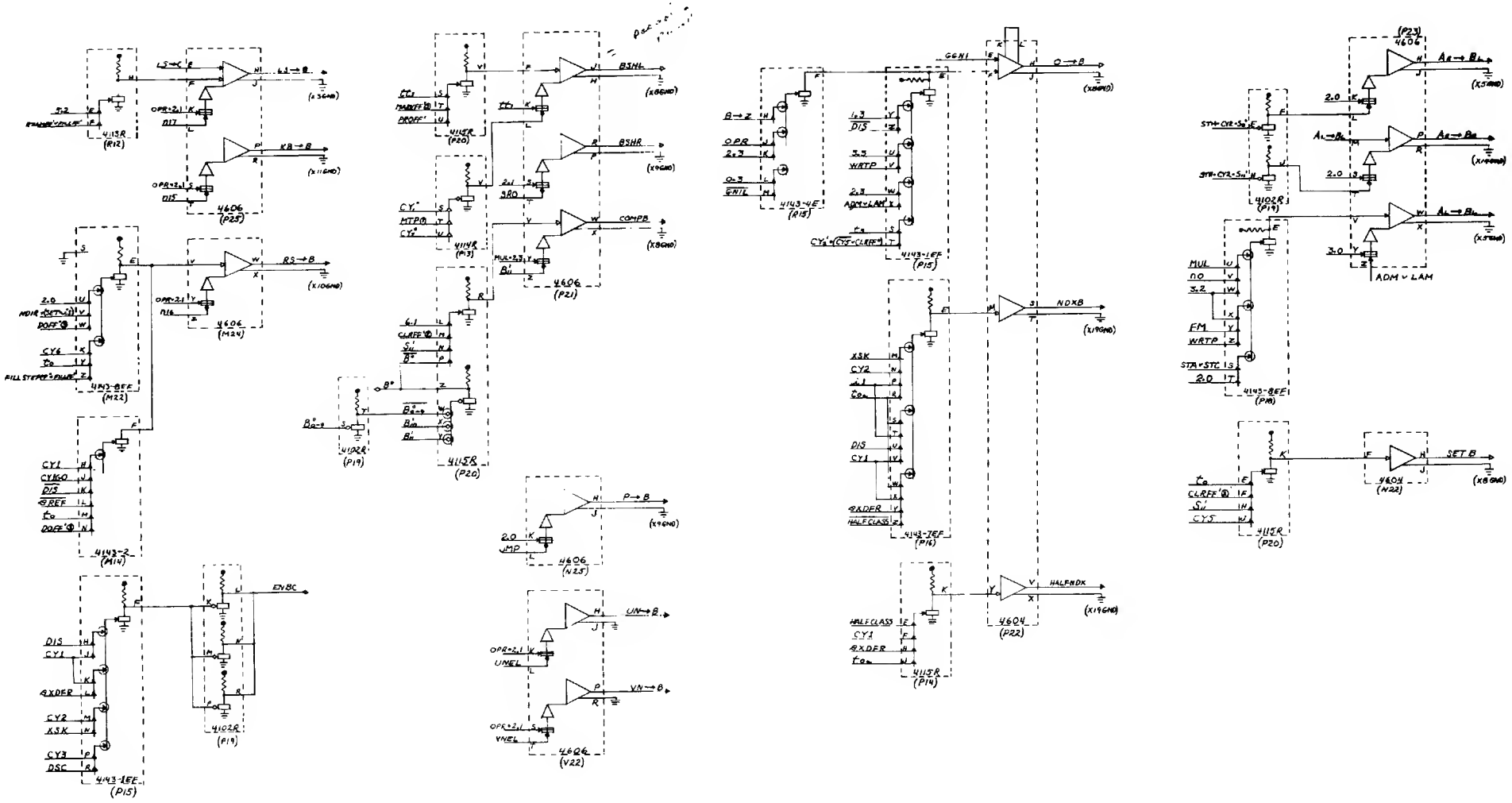
1007	$TP_0 - TP_1$
1007	TP0 – TP3
1026	WPTP
1014	$Z_0 - Z_{11}$



1007	0.0 - 4.3
1020	ADM ∨ LAM
1014	B → Z
1021	B_{0-9}
1011	$B_0 - B_9$
1020	BREF
1020	BXDFR
1018	CLRFF
1007	$CY_0 - CY_3$
1020	$CY_2' \cdot (\overline{CY5} \vee CLRFF^0)$
1007	CY0 — CY6
1008	CY1GO
1018	DOFF
1018	$EDAMFF' \vee FILLFF'$
1018	$FILLSTEPFF' \vee FILLFF'$
1024	FM
1008	GGNI
1005	GNIL
1020	HALFCLASS
1012	$L0 - L1$
1020	INSTRUCTIONS ϕ
1020	INSTRUCTIONS ϕ
1012	LS → C
1018	MARKFF

1020	MUL · 2.3
1012	nO — n17
1020	NOIR ∨ (SET · L1)
1020	OPR · 2.1
1018	PROFF
1013	$S_0 - S_N$
1020	STA ∨ STC
1020	$STN \cdot CY2 \cdot S_0'$
1020	$STN \cdot CY2 \cdot S_N'$
1007	$t_0 - t_3$
1007	t_{0n}
1023	$tt_0 - tt_3$

1026 | WRTP



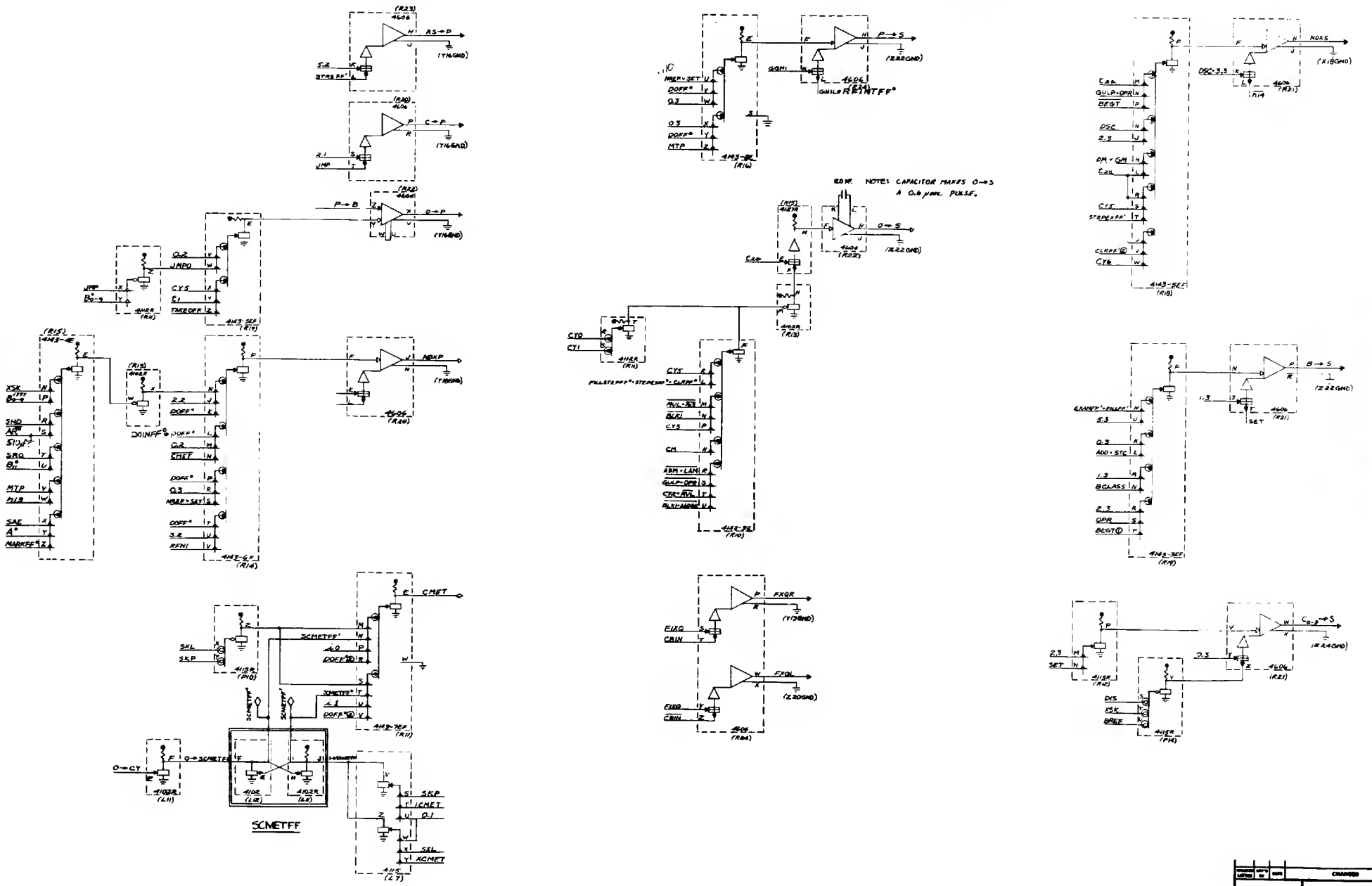
					DRAWING
				LINC	B REGISTER CONTROL LOGIC
				SIZE	
				DATE	1016

1007	0.0 – 6.3
1008	0 → CY
1021	A°
1020	ADM + STC
1020	ADM + LAM
1021	AR°
1011	$B_0 - B_4$
1031	B^{0-9}_{0-9}
1021	B^{1777}_{0-9}
1030	BCLASS
1020	BEGT ◆
EXT.	BEGT ◆

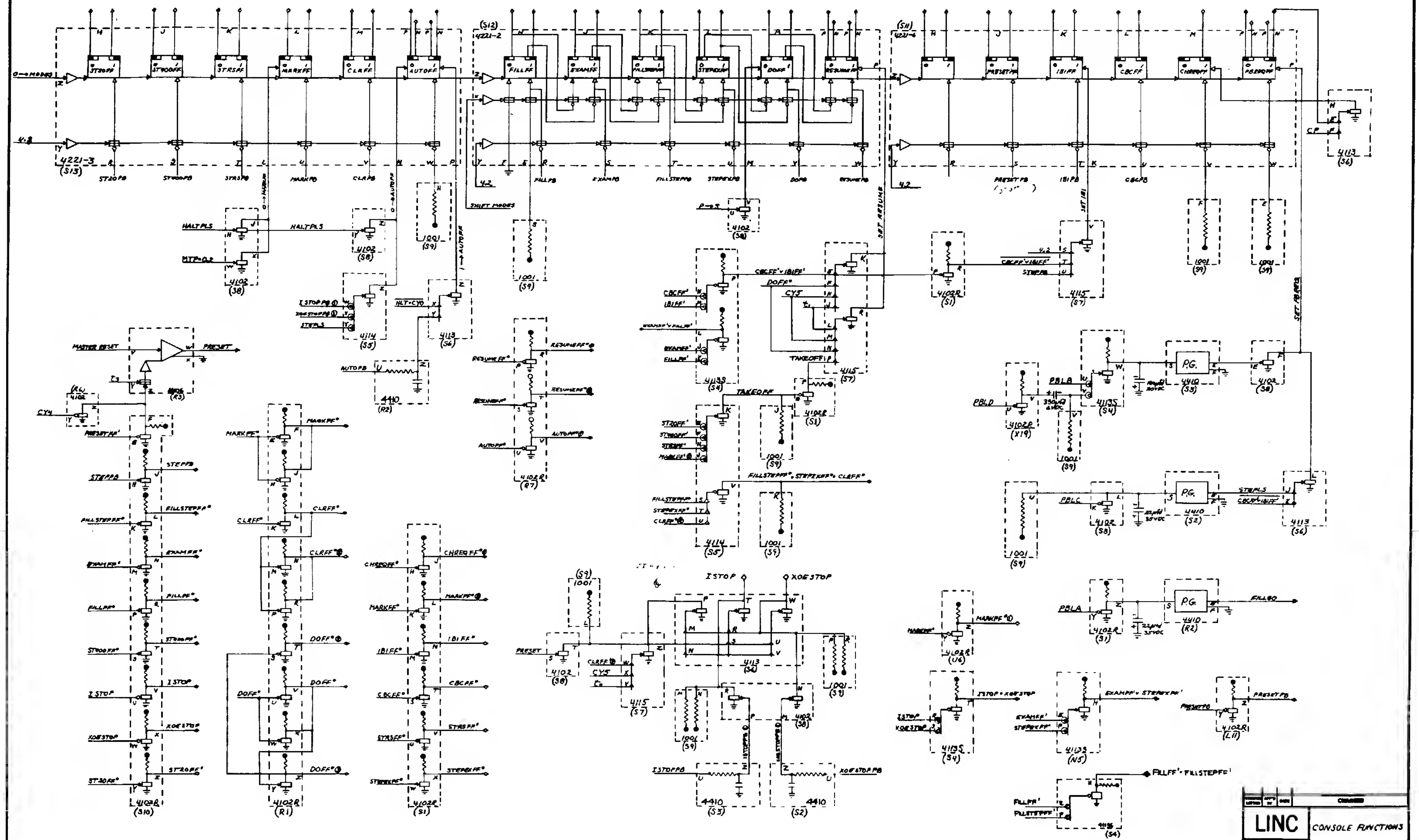
1036	BLKI
1026	BLKI · AADDK
1020	BREF
1026	CBIN
1018	CLRFF
1024	CM ◆
1007	CY0 – CY6
1020	CY1 · MUL
1036	DM + GM
1018	DOFF
1020	DSC · 3.3
1018	EXAMFF' + FILLFF'

1018	FILLSTEPFF° · STEPEXFF° · CLRFF°
1015	FIXQ
1009	GGNI
1009	GNIL
1020	GULP · OPR
1012	i0 – i1
1021	ICMET
1012	INSTRUCTIONS ◆
1030	INSTRUCTIONS ◆
1018	MARKFF
1009	MUL · n13
1012	n0 – n17

1030	NREF + SET
1016	P → B
1026	RFNI
1018	STEPEXFF
1018	STRSFF
1007	$t_0 - t_3$
1019	t_{3a}
1018	TAKEOFF
1021	XCMET
1021	DOINFF
1020	RFINTFF



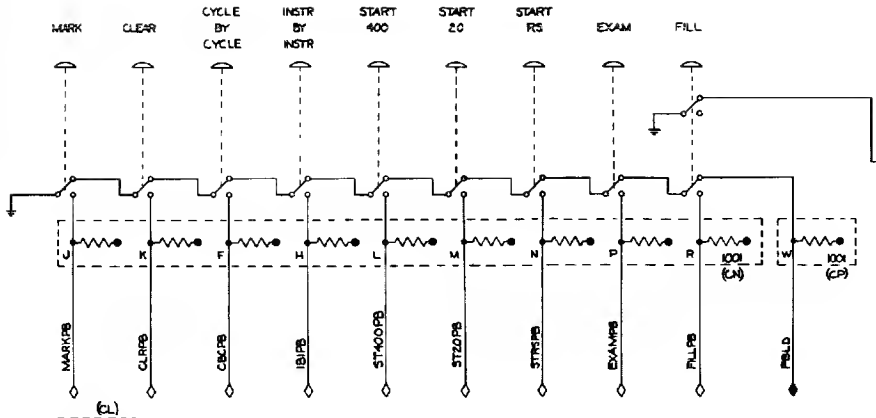
1007	0.0 – 6.3	1009	HALT-CYO	EXT.	ST40PB
1008	0 → MODES	EXT.	IBIPB	EXT.	STEPPB ◆
EXT.	AUTOPB	EXT.	ISTOPPB	EXT.	STEPEXPB
EXT.	CBCPB	EXT.	MARKPB	EXT.	STRSPB
EXT.	CLRPB	1007	MASTER RESET	1007	$t_0 - t_3$
1007	CP	1026	MTP-0.2	EXT.	XOESTOPPB
1007	CYO-CY6	1017	P→S		
EXT.	DOPB	EXT.	PRESETPB ◇		
EXT.	EXAMPB	EXT.	PBLA — PBLD		
EXT.	FILLPB	EXT.	RESUMEPB		
EXT.	FILLSTEPPB	1008	SHIFT MODES		
1009	HALTPLS	EXT.	ST20PB		

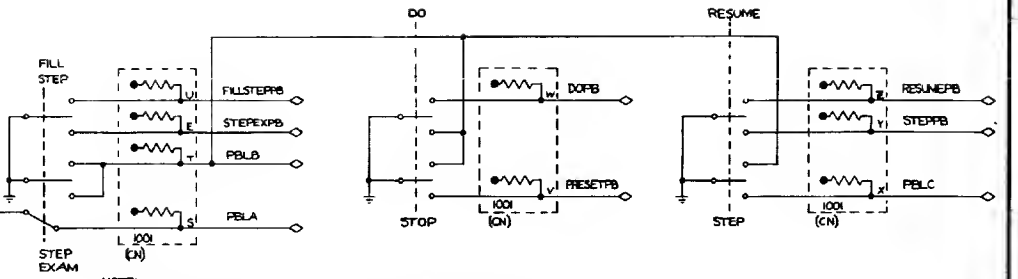


LINC

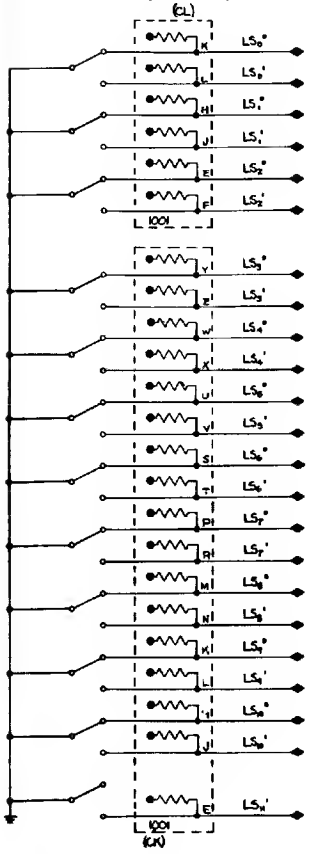
CONSOLE FUNCTIONS

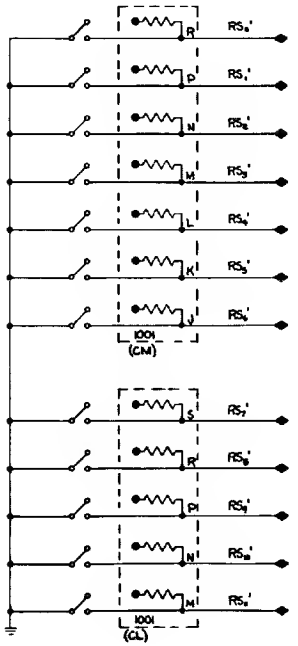
1018

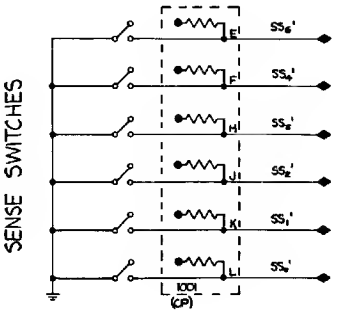


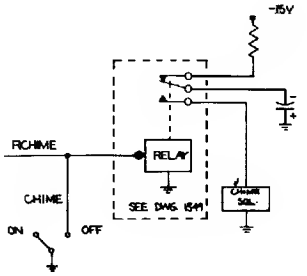


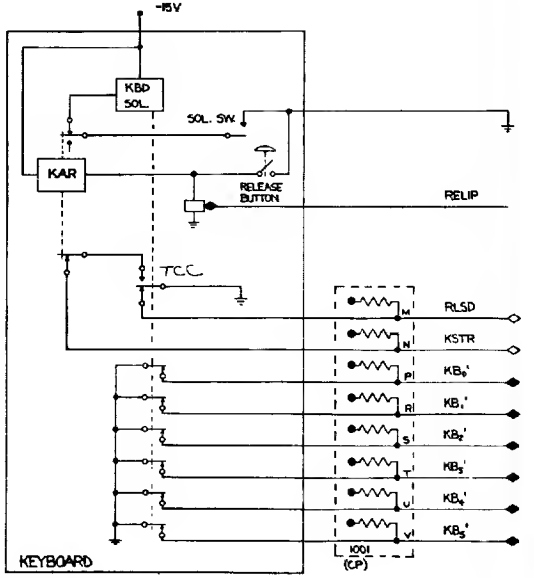
NOTE:
IN THE ABOVE LEVER SWITCHES, THE CONTACT SPRINGS ARE ARRANGED SO THAT THE PBLB LEVEL OCCURS AFTER STEPEXPB, FILLSTEPPB, PRESETPB, DOPB, RESUMEPB; AND PBLC OCCURS AFTER STEPPB. PBLA GOES TO GND ONLY ON RELEASE OF FILLSTEP OR FILL.











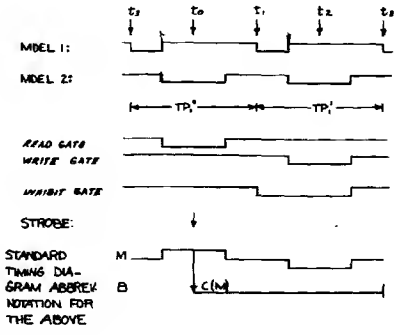
KEYBOARD SEQUENCE:
1. WHEN KEY IS STRUCK, 6 BIT CODE APPEARS ON KB_0 - KB_5
2. KSTR LINE GOES TO GND.
3. KB→B PULSE READS 6 BIT CODE INTO B AND TURNS ON RELIPFF.
4. RELIP OPERATES KAR, RELEASING KBD SOL.
5. RLSD CLEARS RELIPFF.

LINC	KEYBOARD AND CONSOLE SWITCH SIGNALS	
DATE	1018A	

1007	0.0 - 4.3
1020	ADM + LAM
1017	B → S
1026	BLK1
1026	BLK1 · C_2^0
1026	(BLK1 · C_2^0) · WRTP
1017	$C_{0-3} \rightarrow S$
1012	$C_0 - C_3$
1018	CLRFF
1007	CY0 - CY6
1034	DM
1018	DOFF

1018	FILLFF' + FILLSTRFF'
1024	GM
1020	INSTRUCTIONS ◆
1008	JMP 8
1020	MBUT ◆
1012	MQ - MI7
1017	NOXS
1020	OPR · GULP
1017	P → S
1018	PRESET
1020	STA · STC
1020	STH · CY3 · S_4^0

1020	STH · CY3 · S_4^1
1009	STOPPED
1007	$t_0 - t_3$
1007	$TP_0 - TP_1$



TYPICAL VALUES

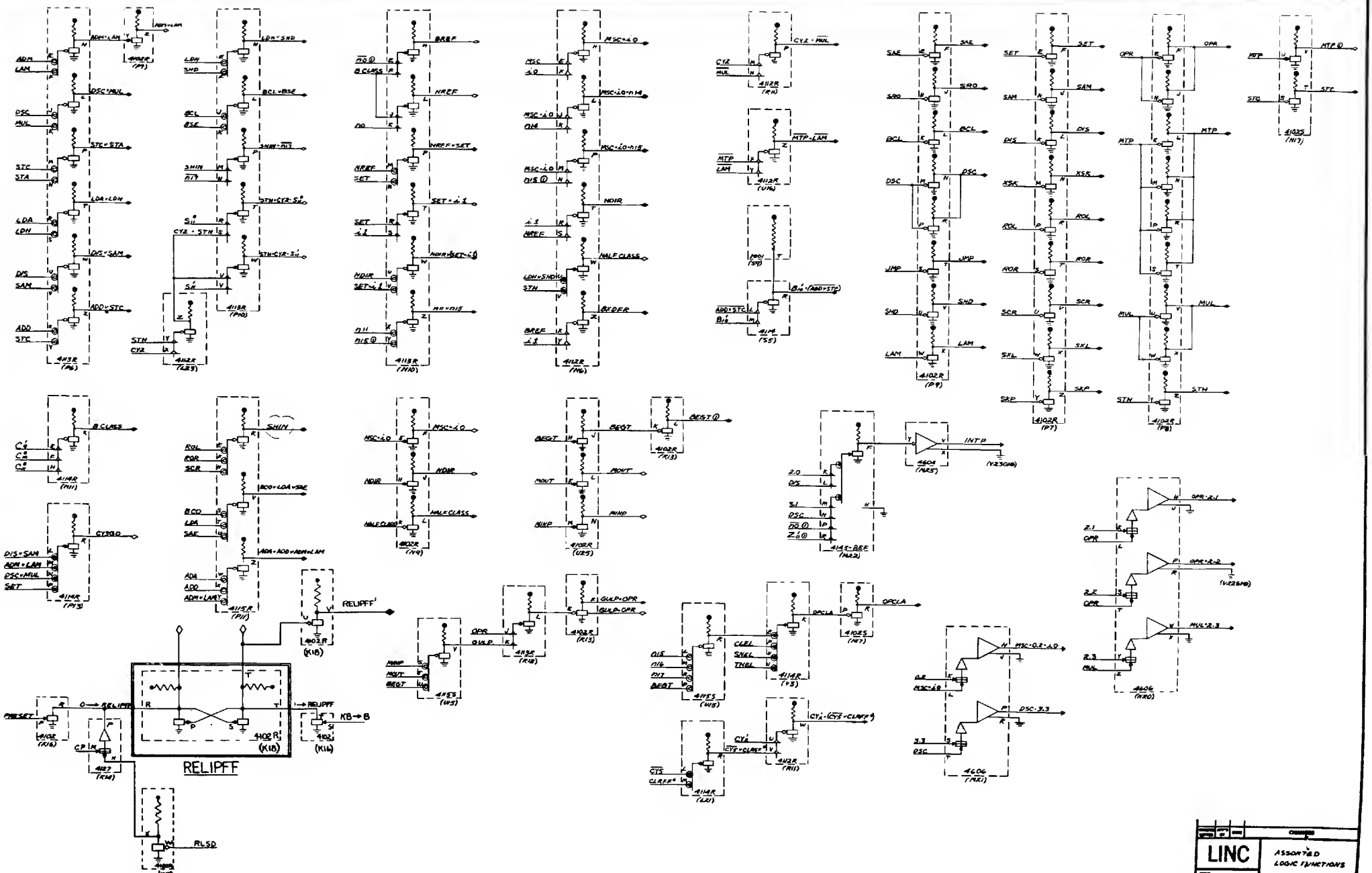
MDEL 1: 0.9 μsec

MDEL 2: 1.8 μsec

LINC	MEMORY CONTROL LOGIC	
DATE	1019	DR.

1007	0.0 - 6.3
EXT.	BEGT ⊕
1012	$C_0 - C_8$
EXT.	CLEL ⊕
1007	CP
1007	$CY_0 - CY_5$
1007	CY0 - CY6
1012	L0 - L1
1012	INSTRUCTIONS ⊕
1014	KB → B
EXT.	MINP ⊕
EXT.	MQLT ⊕

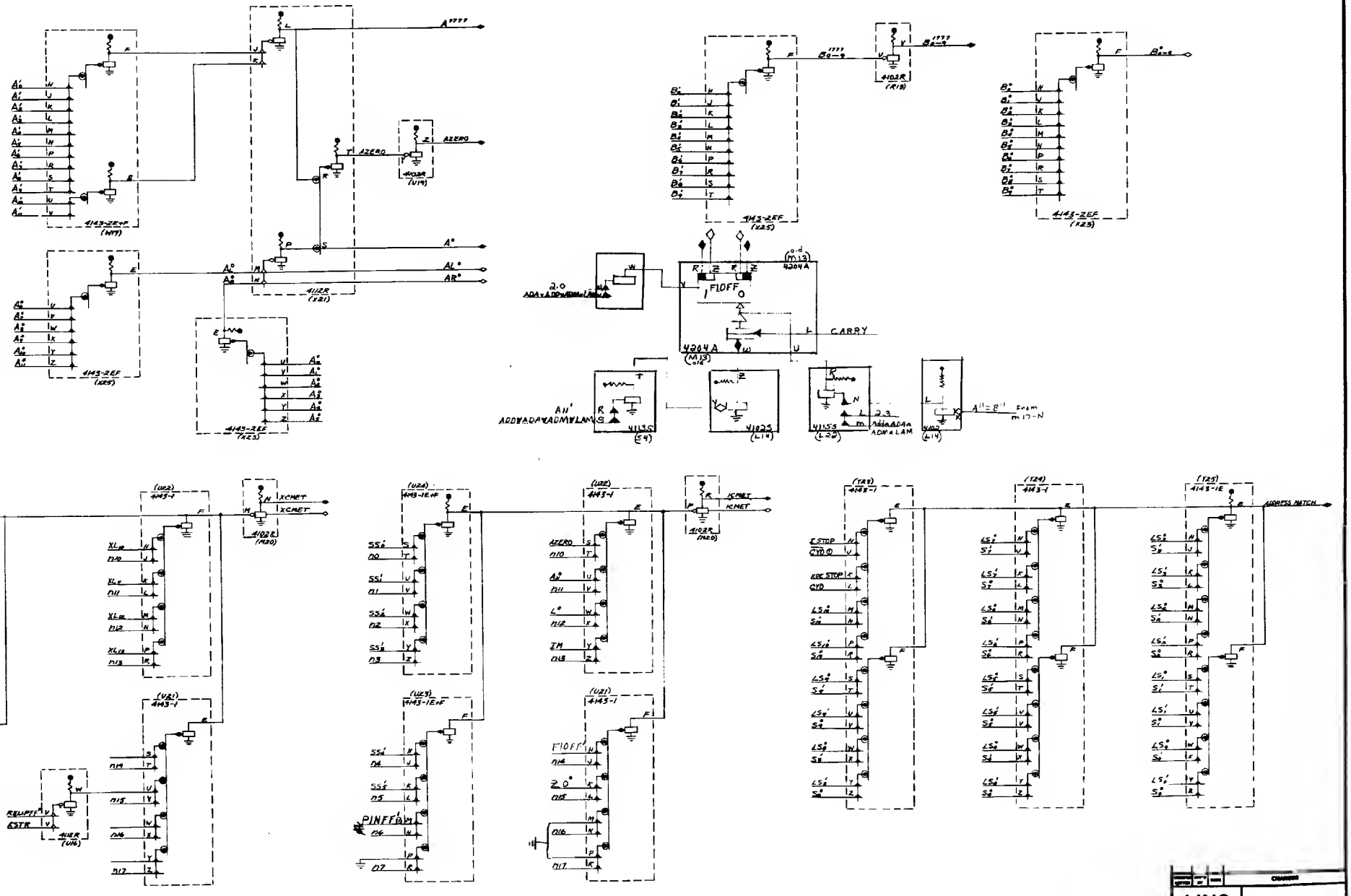
1012	H0 - H17
1013	PRESET
EXT.	RLSD ⊕
1013	$S_0 - S_8$
EXT.	SNEL ⊕
EXT.	TNEL ⊕
1014	$Z_0 - Z_8$



LINC	ASSORTED LOGIC FUNCTIONS
DATE	1020

1010	$A_0 - A_{11}$
1011	$B_0 - B_{11}$
1007	CYD - CY6
1024	IM
1018	ISTOP
EXT.	KSTR 4
1014	L
EXT.	$LS_0 - LS_{11}$
1012	m0 - m17
1026	RELIPFF
1013	$S_0 - S_{11}$
EXT.	$SS_0 - SS_{11}$

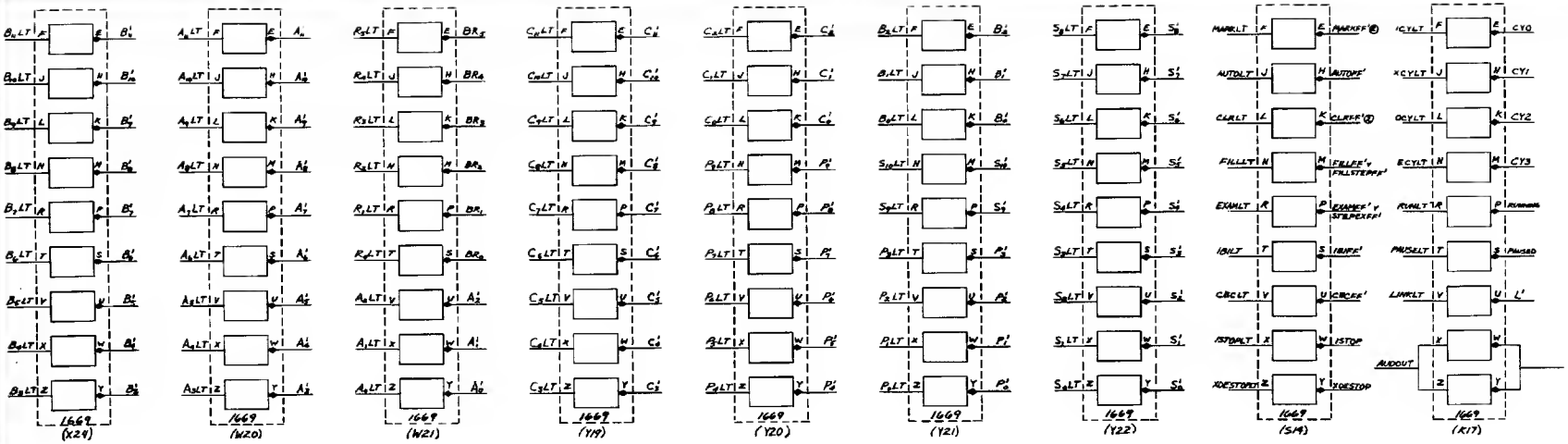
EXT.	$XL_0 - XL_{13}$
1015	XOFSTOP

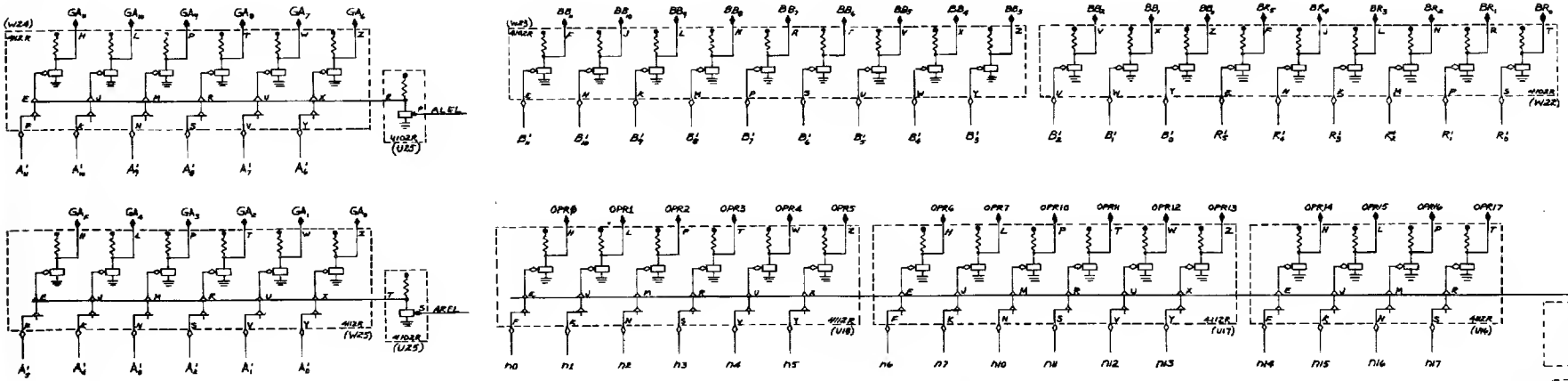


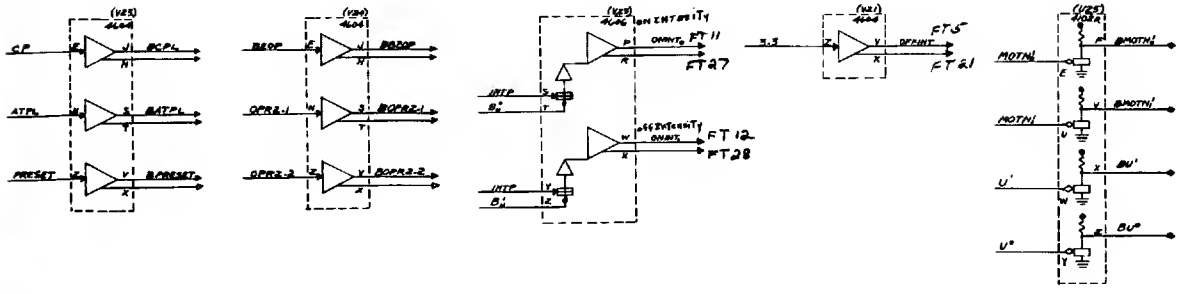
1007	0.0 - 6.3
1016	$A_0 - A_{11}$
EXT.	ALEL ↑
EXT.	AREL ↑
1007	ATPL
1015	AUTOFF
1011	$B_0 - B_{11}$
1009	BEOP
1013	$C_0 - C_{11}$
1015	CBCFF
1018	CLRFF
1007	C.P

1007	CY0 - CY6
1017	EXAMFF' v STEPEXFF'
1018	FILLFF' v FILLSTEPFF'
1009	GGN1
1015	IBIFF
1020	INSTRUCTIONS ↑
1020	INTP
1015	ISTOP
1014	L
1018	MARKFF
1035	$MOTN_0 - MOTN_7$
1012	$H0 - H17$

1020	OPR - 2.1
1020	OPR - 2.2
1013	$P_0 - P_{11}$
1009	PAUSED
1015	PRESET
1014	$R_0 - R_{11}$
1009	RUNNING
1013	$S_0 - S_{11}$
1035	U
1015	XOESTOP

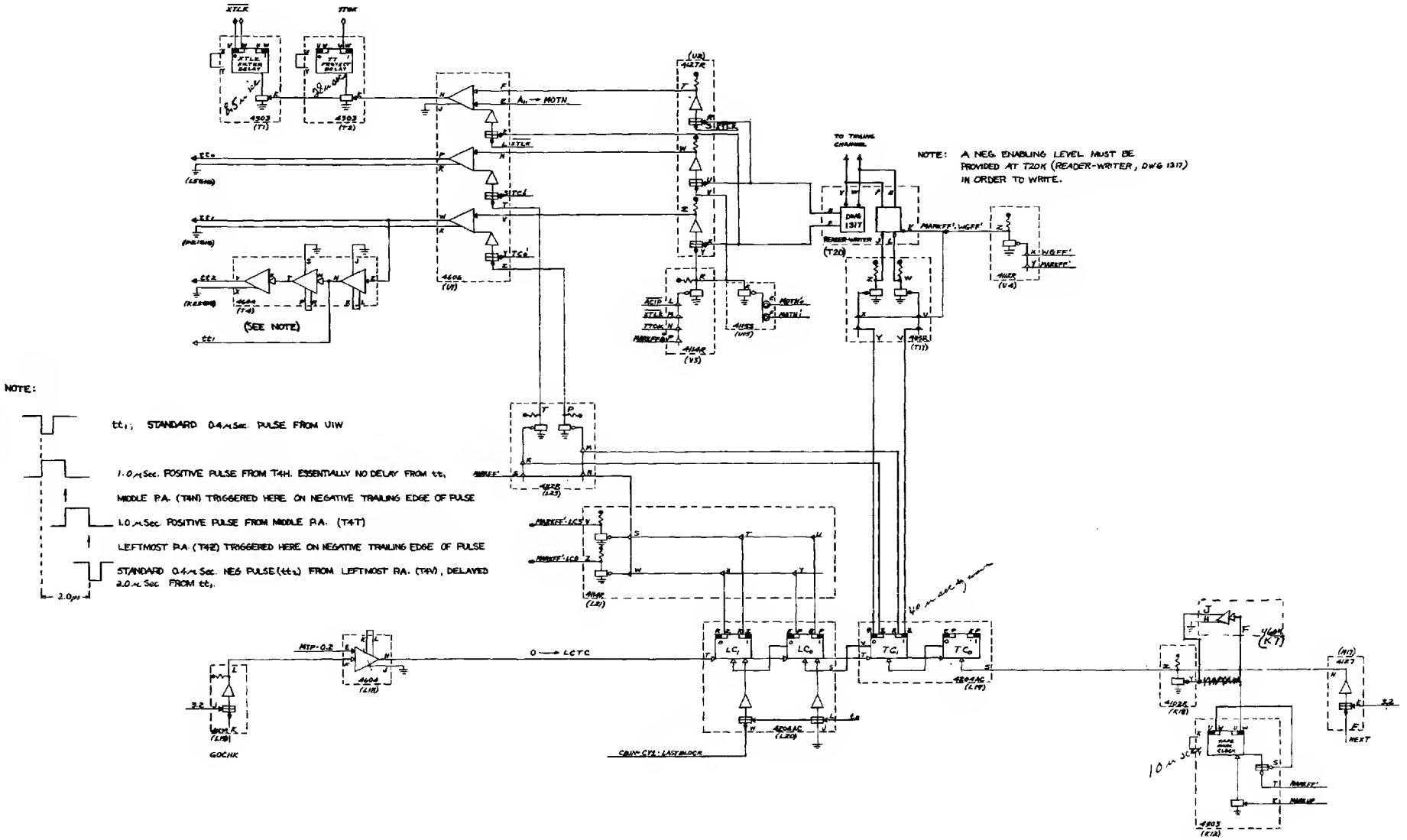






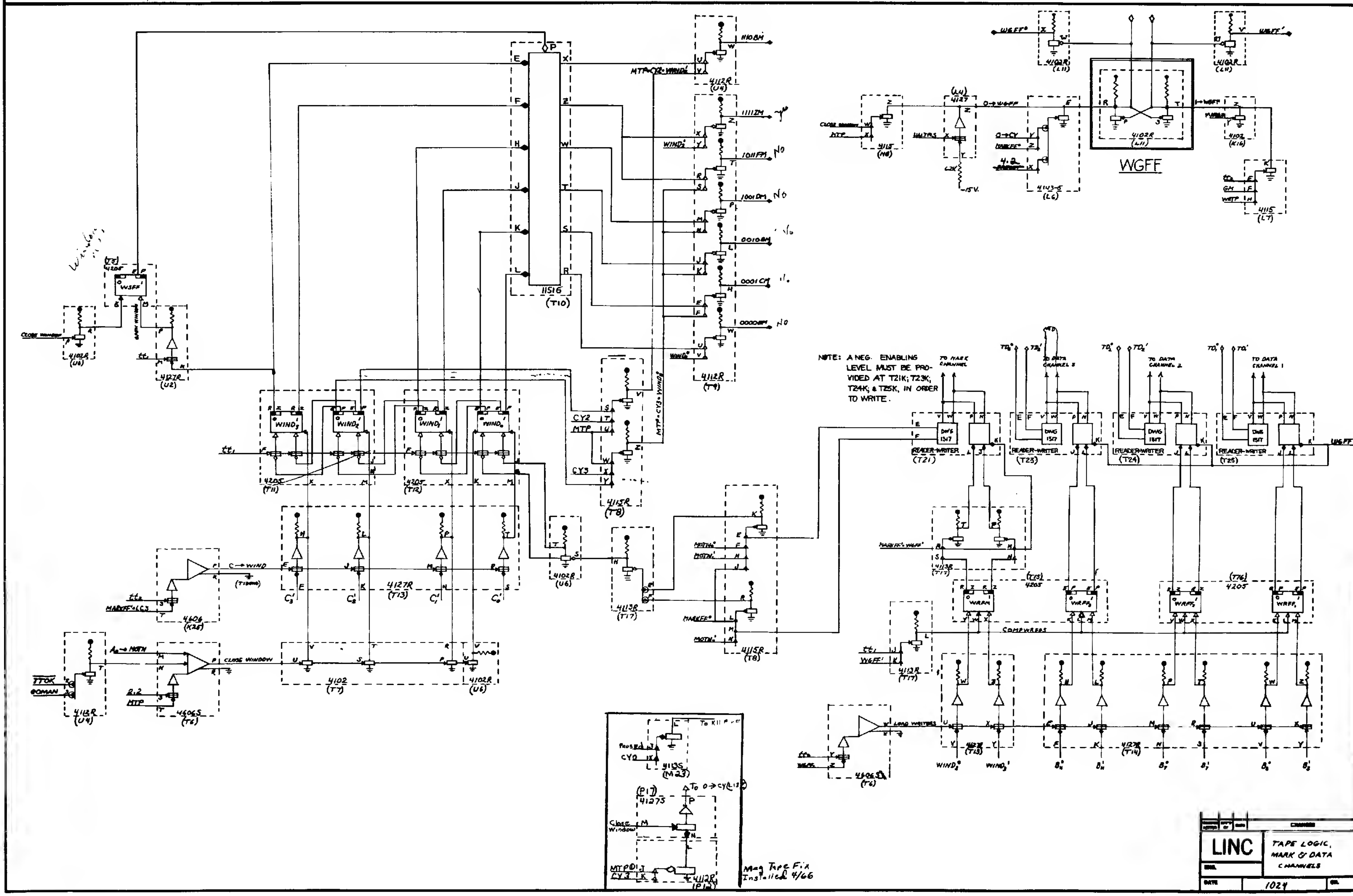
LINC — OUTPUT DRIVERS AND BUFFERS — 1022

1007	0.0 – 6.3
1825	$A_H \rightarrow$ MOTN
1825	ACIP
1826	CBIN · CY1 · LAST BLOCK
1018	MARKFF
1826	MARKUP
1825	$MOTN_0$ – $MOTN_1$
1026	MTP · 0.2
1007	t_0 – t_3
1024	WGFF



LINC	TAPE TIMING CHANNEL LOGIC	
DATE	1023	

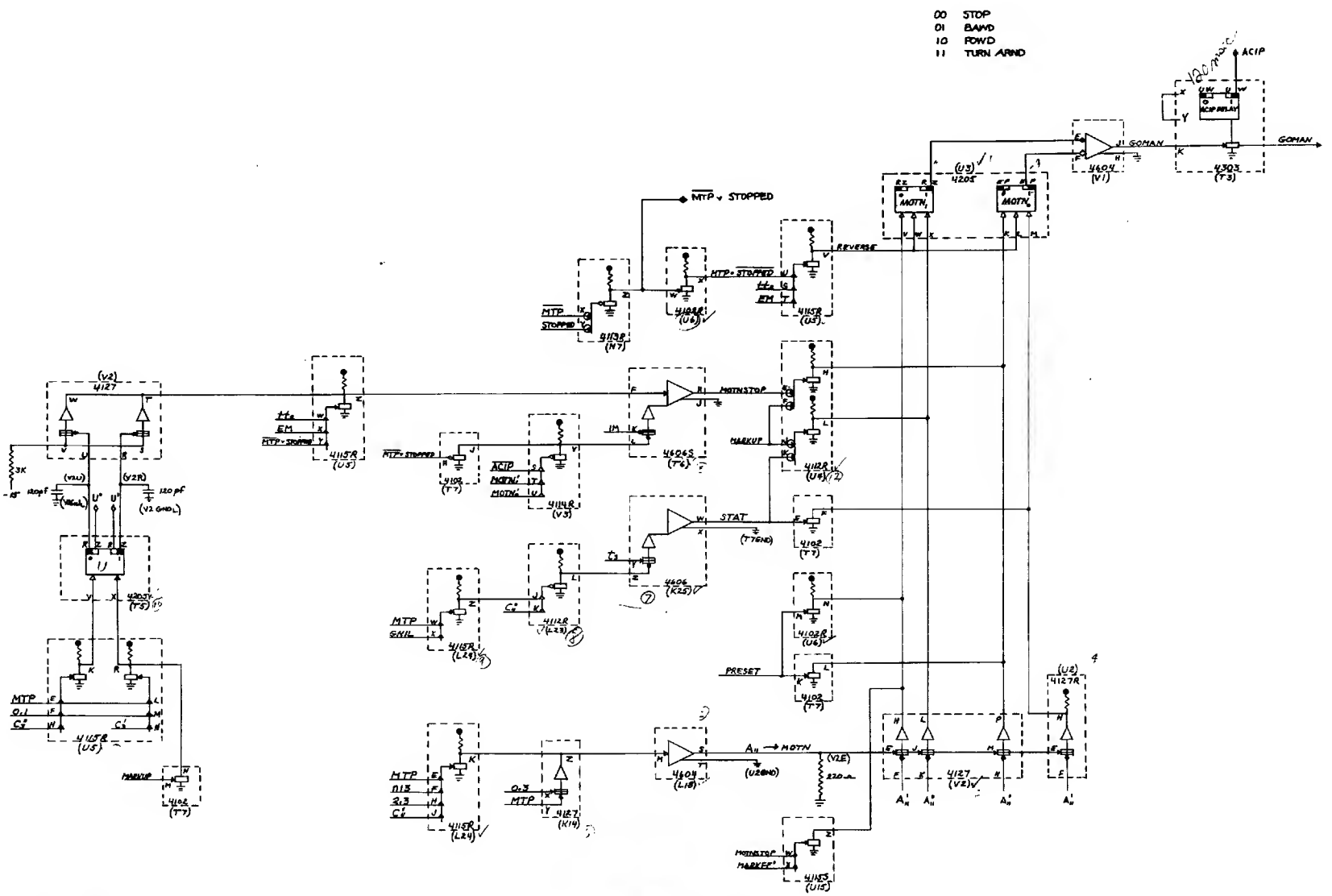
1007	0.0 - 6.3
1008	0 → CT
1035	A_H → MOTN
1011	B_0 - B_H
1012	C_0 - C_H
1025	GOMAN
1009	HALTPLS
1020	INSTRUCTIONS ♦
1015	MARKFF
1023	MARKFF'·LC3
1033	MARKFF'·WGFF'
1036	MARKUP
1035	$MOTN_0$ - $MOTN_1$
1018	PRESET
1023	tt_0 - tt_2
1023	TTOK
1126	WRTP



1007	$Q_0 - Q_3$
1010	$A_0 - A_{11}$
1012	$C_0 - C_{11}$
1024	EM
1008	GNIL
1024	IM
1020	INSTRUCTIONS ◆
1018	MARKFF
1026	MARKUP
1012	n0 - n17
1018	PRESET
1049	STOPPED

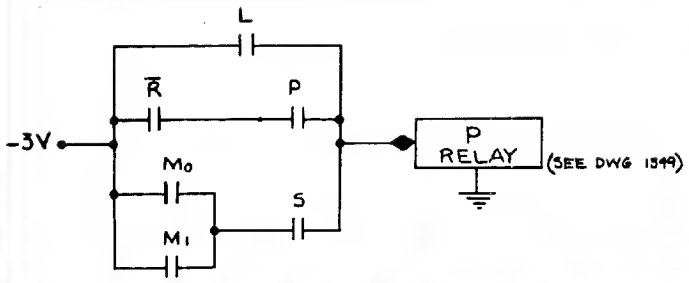
1007	$\bar{Q}_0 - \bar{Q}_3$
1033	$\bar{EE}_0 - \bar{EE}_{11}$

00 STOP
01 BAWD
10 FOWD
11 TURN ARND

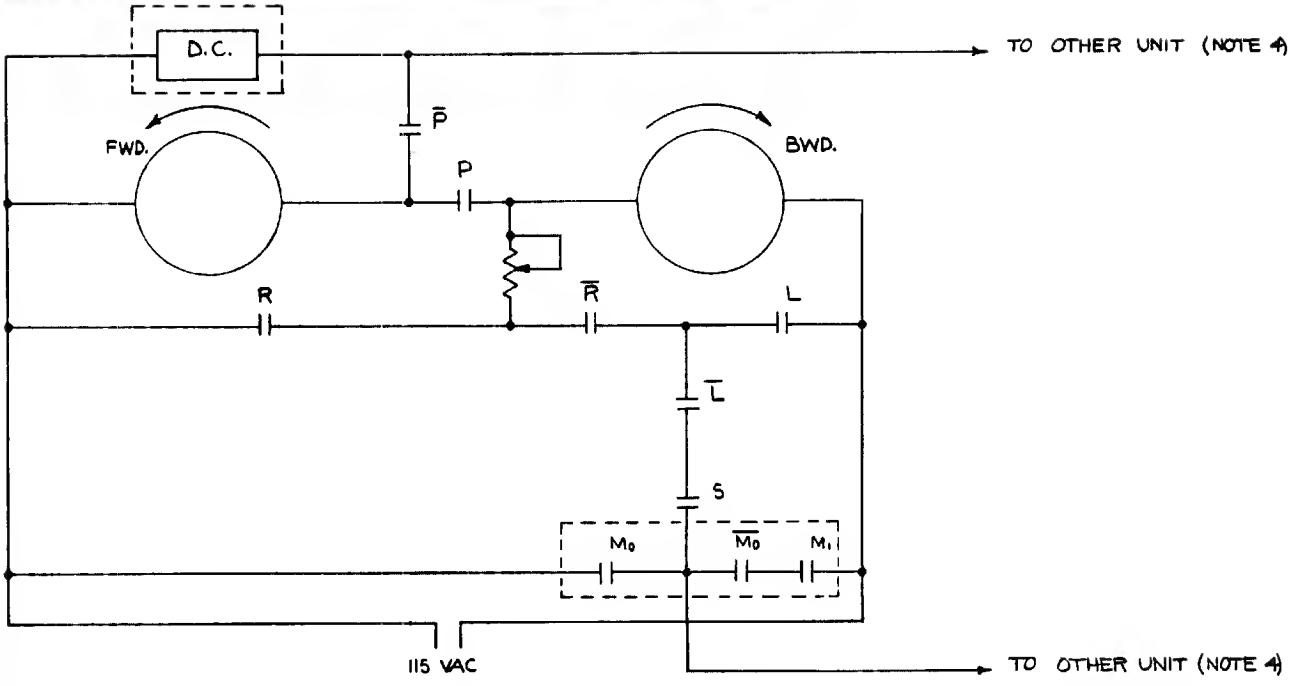


U3 ✓
V2 ✓
L18 ✓
T5 ✓
U4
U6

LINC	TAPE MOTION CONTROL LOGIC
DATE	1025



POWER RELAY (P) LATCHING CONTROL (NOTE 1)



1. POWER RELAY (P) WHENEVER A CLOSED PATH CONNECTS -3 VOLTS TO THE P RELAY CONTROL, THE P CONTACTS CLOSE. ONCE CLOSED, THEY CAN BE OPENED AGAIN ONLY BY OPENING THE $\overline{R}$ CONTACT, i.e. BY PRESSING THE R BUTTON.
2. CONTACT NOTATION: —|X|— A CONTACT WHICH IS CLOSED WHEN CONDITION "X" EXISTS.
   —|$\overline{X}$|— A CONTACT WHICH IS OPEN WHEN CONDITION "X" EXISTS.
3. "L" = LEFT BUTTON
   "R" = RIGHT BUTTON
4. ONLY ONE OF THE TWO UNITS IS SHOWN, AS THEY ARE ESSENTIALLY IDENTICAL. DOTTED LINES INDICATE SECTIONS SHARED BY THE TWO UNITS, i.e. THERE IS BUT ONE D.C. SUPPLY AND ONE PAIR OF MOTION RELAYS. IN ADDITION TO THE 115 VOLT LINE, THE TWO INDICATED LINES ARE CONNECTED TO THE OTHER UNIT. UNITS OPERATE INDEPENDENTLY SO FAR AS PUSH BUTTONS ARE CONCERNED. EACH UNIT HAS A SELECTION RELAY (S), WHICH, WHEN ACTIVATED, CONNECTS CONTROL TO THE M_0 AND M_1 RELAYS. THESE MOTION RELAYS ARE CONTROLLED BY BMOTN$_0$' ◆ AND BMOTN$_1$' ◆ LEVELS DERIVED FROM THE MOTN$_0$ AND MOTN$_1$ FLIP-FLOPS IN THE CABINET. (SEE DWG. 1025) NOTE THAT THE SUBSCRIPTS DO NOT REFER TO THE UNIT, i.e. BOTH FLIP-FLOPS ARE REQUIRED TO CONTROL THE MOTION OF EITHER UNIT SELECTED. ONLY ONE UNIT WILL HAVE ITS SELECTION RELAY ACTIVATED AT ANY ONE TIME.
   THE VARIOUS STATES ARE:

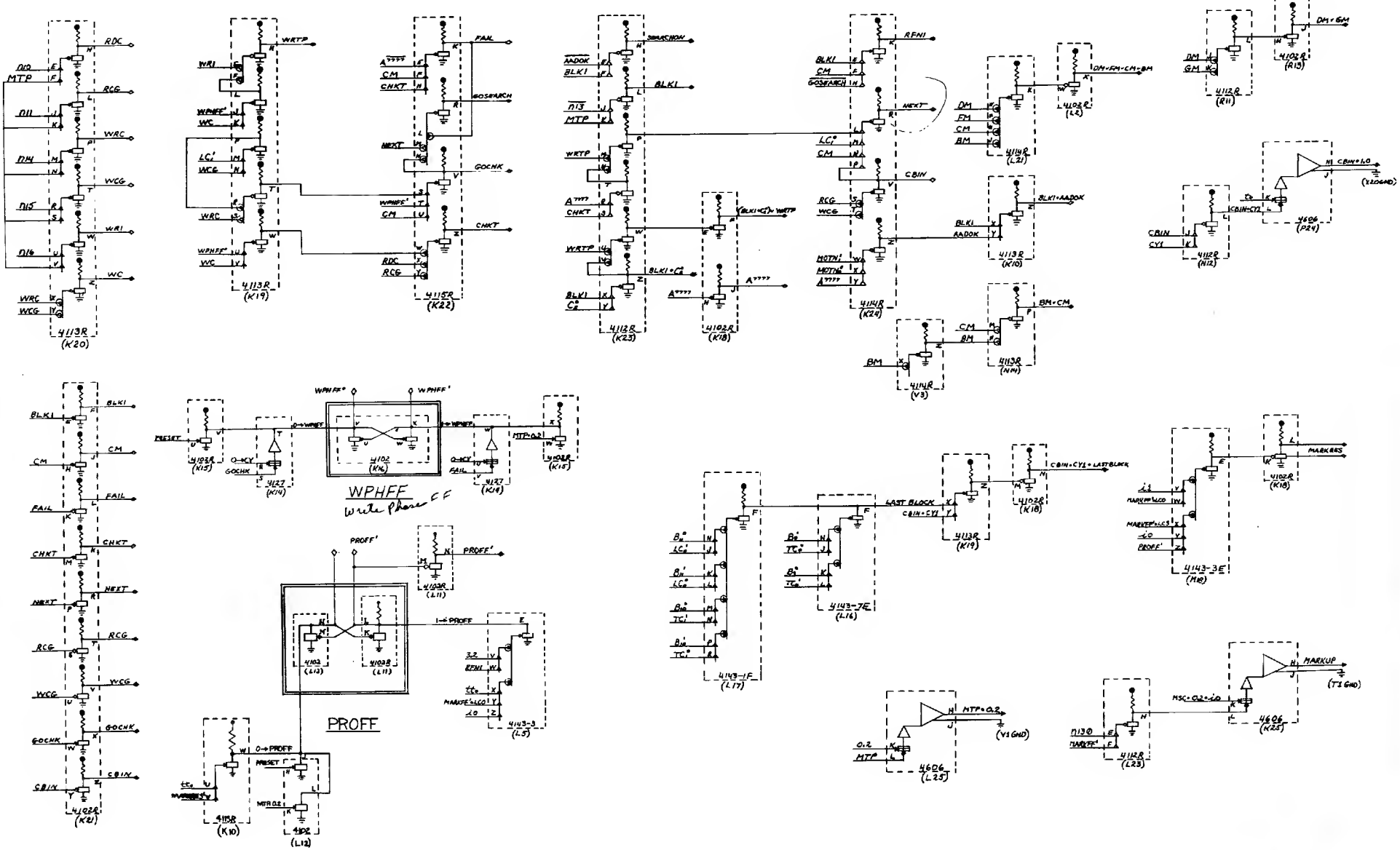
MOTN$_1$	MOTN$_0$	LEFT MOTOR	RIGHT MOTOR	RESULTANT MOTION
0	0	HALF VOLTAGE	HALF VOLTAGE	STOP
0	1	SHUNTED	FULL VOLTAGE	BACKWARD
1	0	FULL VOLTAGE	SHUNTED	FORWARD
1	1	SHUNTED	FULL VOLTAGE	BACKWARD

5. THE VARIABLE RESISTOR ACTS AS A VOLTAGE DIVIDER SO THAT RATHER THAN COMPLETELY SHUNTING ONE MOTOR, AND APPLYING FULL VOLTAGE TO THE OTHER, A SMALL PART OF THE VOLTAGE MAY BE APPLIED TO THE TRAILING MOTOR. THIS PERMITS PROPER ADJUSTMENT OF TAPE TENSION.

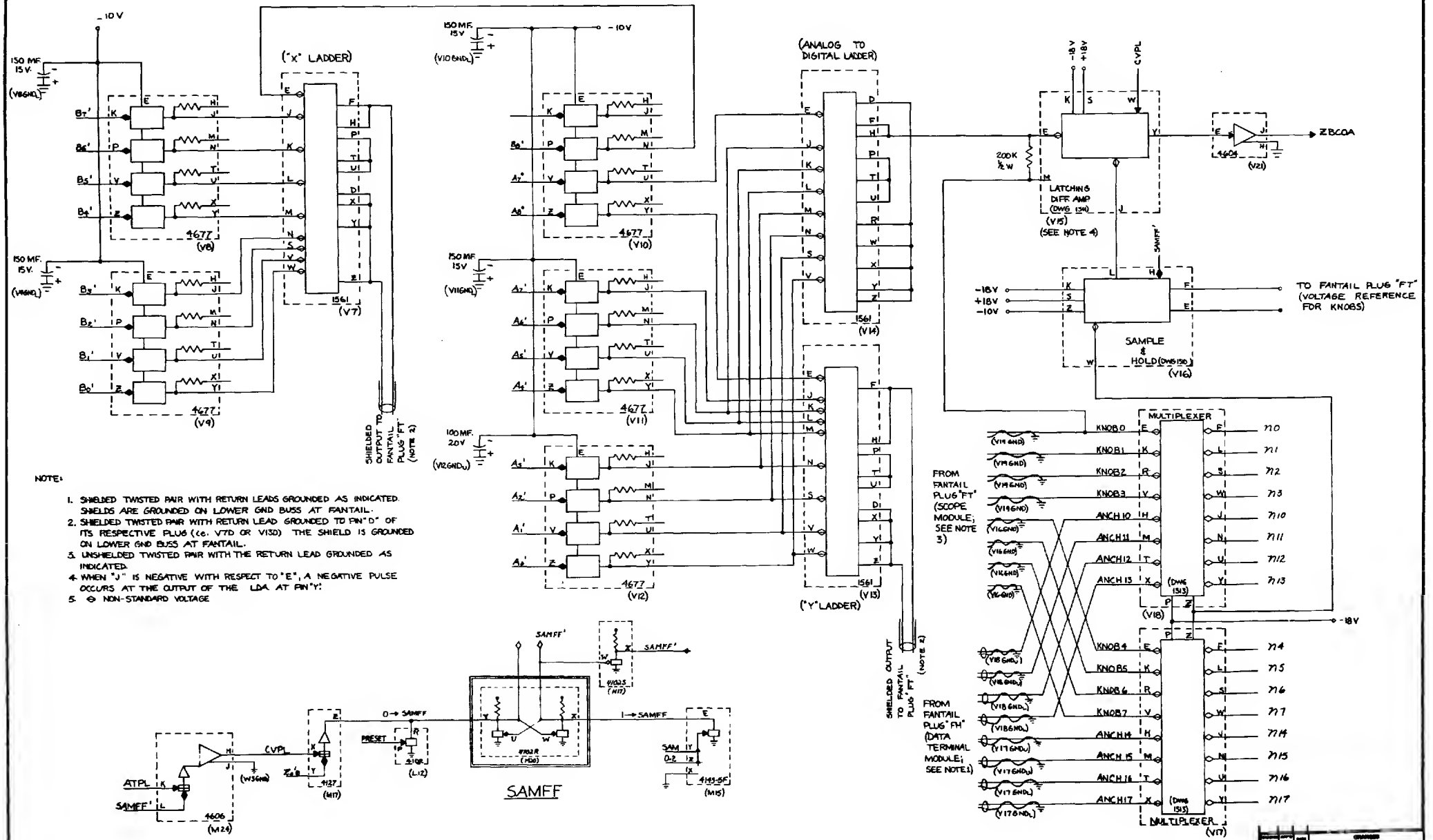
LINC
TAPE UNITS
MOTOR POWER
CONTROL NETWORK
1025A

1007	0.0 - 4.3
1008	0 → CY
1021	A^{7777} ϕ
1024	BM ϕ
1012	$C_0 - C_8$
1029	CM ϕ
1007	CY0 - CY6
1024	DM
1029	FM
1032	INSTRUCTIONS ϕ
1033	$LC_0 - LC_4$
1035	$MOTN_0 - MOTN_4$

1012	$n0 - n17$
1018	PRESET
1007	$t_0 - t_3$
1033	$EE_0 - TT_4$



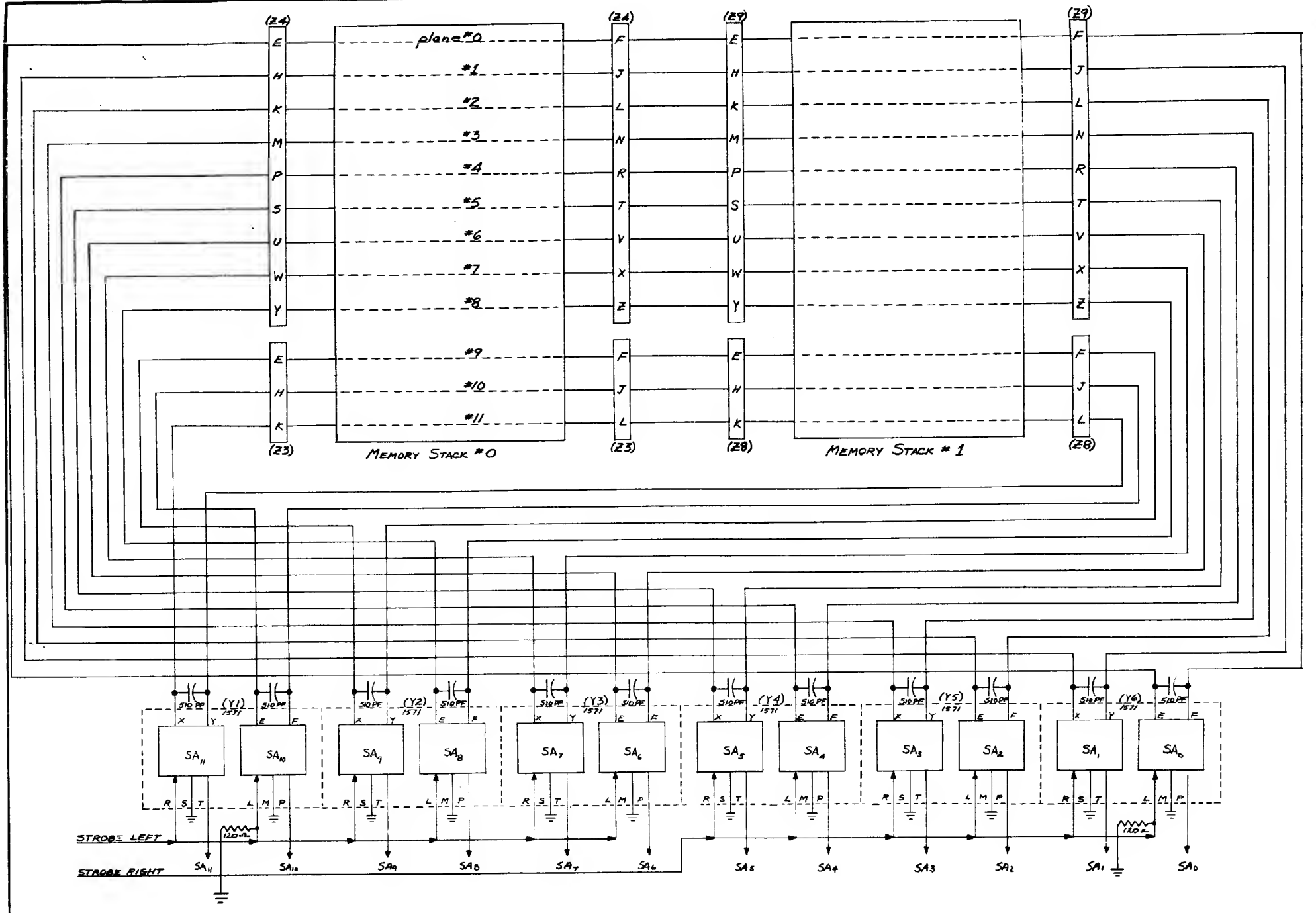
1007	0.0 - 6.3
1010	$A_0 - A_6$
EXT.	ANCH 10 - ANCH 17
1007	ATPL
1011	$B_0 - B_6$
1020	INSTRUCTIONS ⊕
EXT.	KNOB 0 - KNOB 7
1012	A0 - A17
1015	PRESET
1014	$Z_0 - Z_6$



NOTE:

1. SHIELDED TWISTED PAIR WITH RETURN LEADS GROUNDED AS INDICATED. SHIELDS ARE GROUNDED ON LOWER GND BUSS AT FANTAIL.
2. SHIELDED TWISTED PAIR WITH RETURN LEAD GROUNDED TO PIN "D" OF ITS RESPECTIVE PLUG (i.e. V7D OR V13D) THE SHIELD IS GROUNDED ON LOWER GND BUSS AT FANTAIL.
3. UNSHIELDED TWISTED PAIR WITH THE RETURN LEAD GROUNDED AS INDICATED.
4. WHEN "J" IS NEGATIVE WITH RESPECT TO "E", A NEGATIVE PULSE OCCURS AT THE OUTPUT OF THE LDA AT PIN "Y".
5. ⊕ NON-STANDARD VOLTAGE

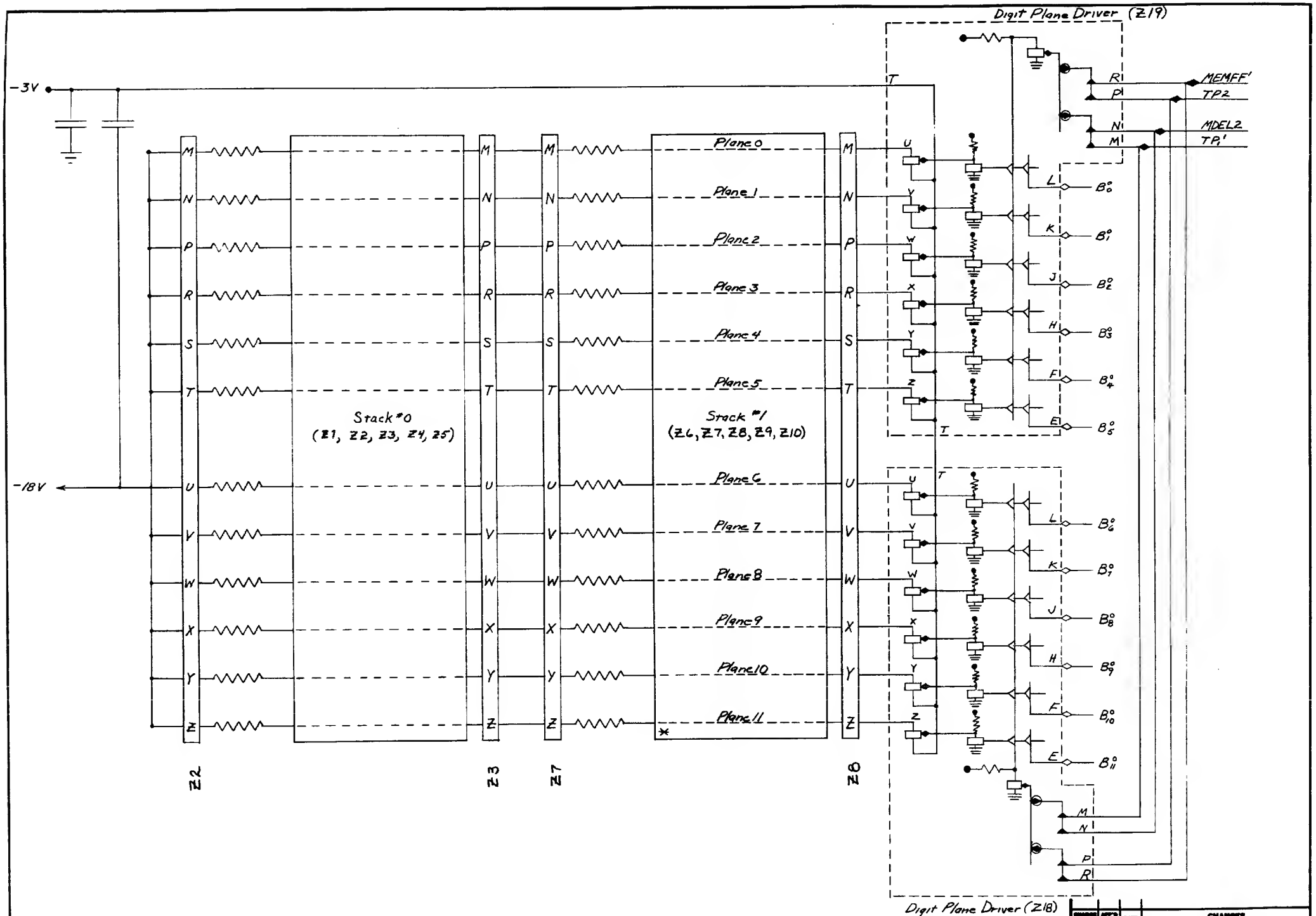
LINC — ANALOG DIGITAL SYSTEM — 1027



NOTE:

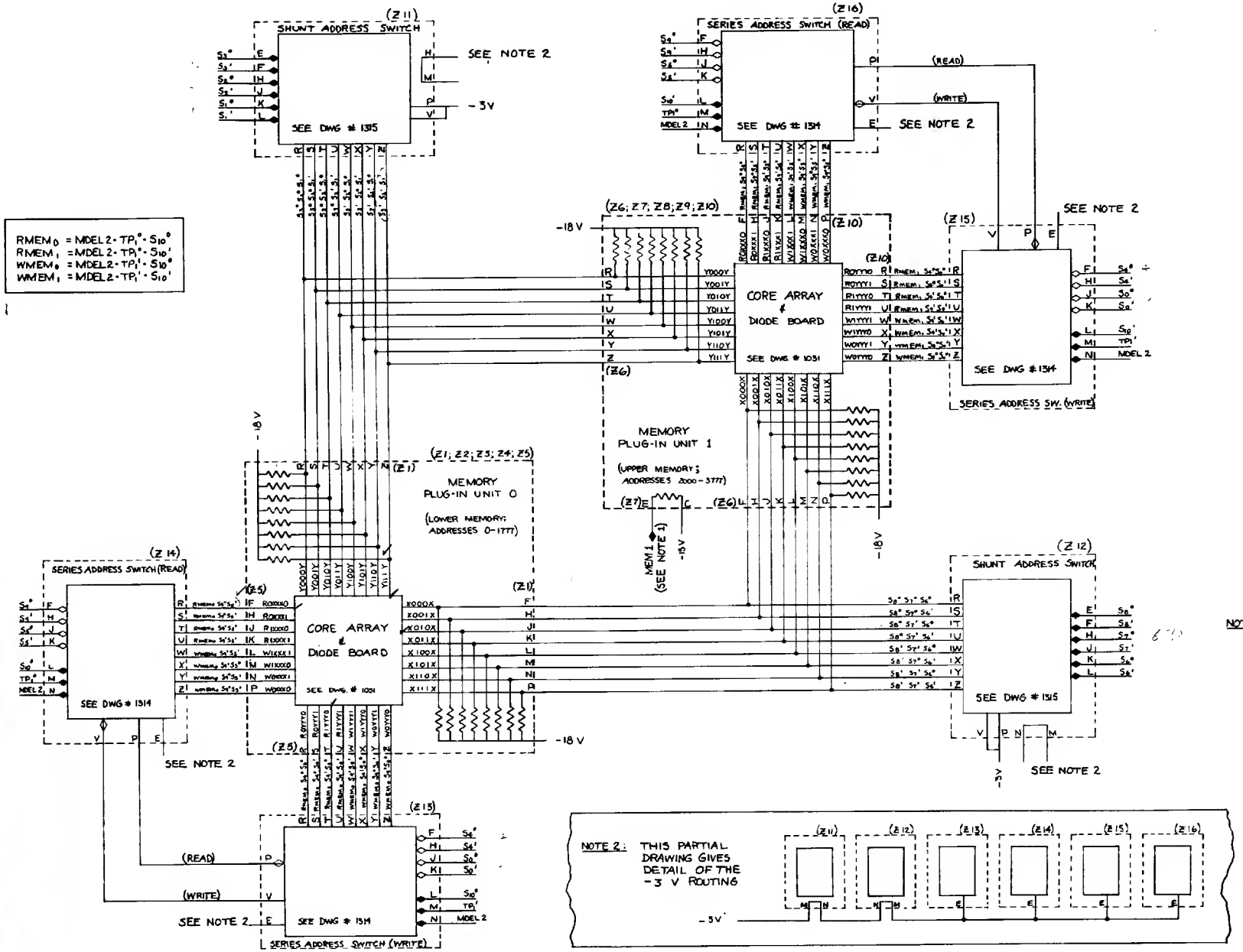
1. A BY PASS CAPACITOR, (100 MFD, 20 V, 20%, SPRAGUE # 1500) IS ATTACHED BETWEEN Y2C (-15 VOLTS) AND Y4 GND$_U$.
2. SLICE LEVELS ARE AVAILABLE ON SENSE AMPLIFIER PINS "U" AND "K" (FOR UPPER AND LOWER AMPS.)
3. EACH SENSE AMPLIFIER INPUT, (PINS X, Y, E, F) HAS A 120Ω RESISTOR TO GROUND.

CHANGES			CHANGES
LINC			MEMORY SENSE LOGIC
ENG.			
DATE	1028		CH.



CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC	MEMORY DIGIT PLANE CONNECTIONS		
ENG.			
DATE	1029		CH.

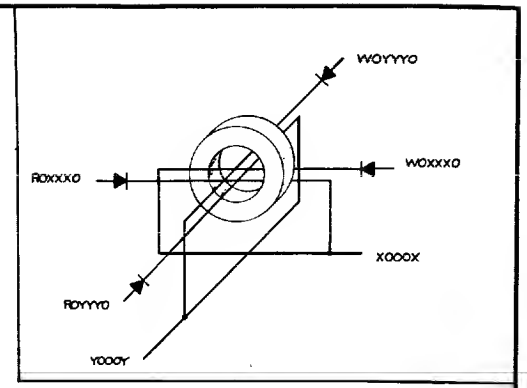
1019 | MDEL 2
1013 | $S_{10} - S_{17}$
1007 | $TP_0 - TP_1$

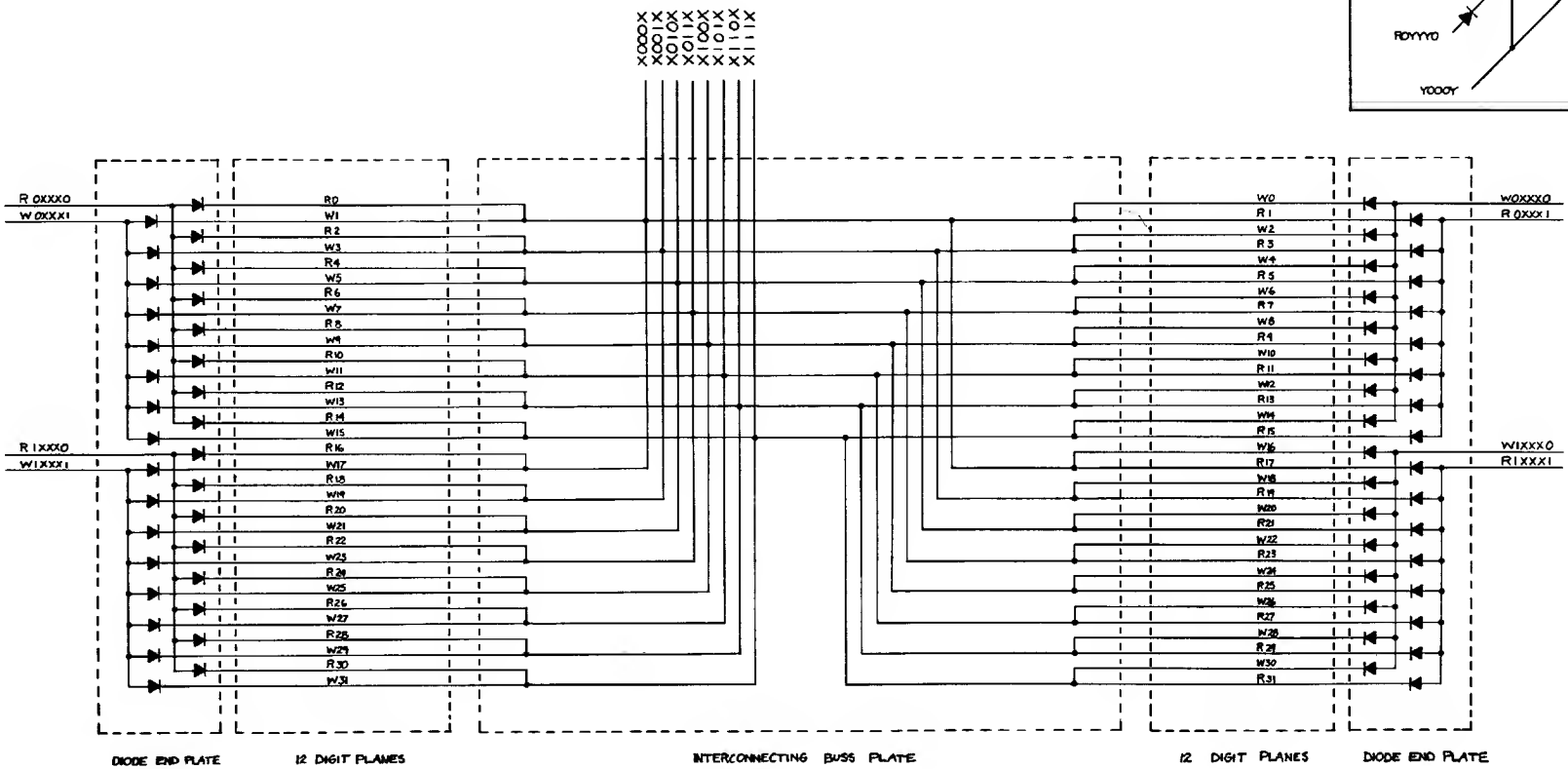


NOTE 1: WHEN A DUMMY STACK PLUG-IN UNIT IS INSERTED, PIN E OF Z7 IS INTERNALLY CONNECTED TO GND.

WHEN MEMORY PLUG-IN UNIT 1 IS INSERTED, PIN E OF Z7 IS INTERNALLY CONNECTED TO -15 V THROUGH A 10KΩ RESISTOR.

LINC | MEMORY ADDRESS SELECTION SYSTEM
DATE | 1030





NOTE 1: EACH CORE HAS TWO X SELECTION AND TWO Y SELECTION LINES RUNNING THROUGH IT. (SEE PICTORIAL ABOVE) THE DIGIT PLANES ARE DRAWN TWICE SCHEMATICALLY SO THIS MAY BE MORE EASILY SEEN.

NOTE 2: THE "Y" MEMORY STACK ADDRESS IS WIRED FROM A SIMILAR SCHEMATIC.

LINC	"X" MEMORY STACK ADDRESS WIRING	
DWG.		
DATE	1031	DR.

FU (MAG TAPES)

NAME		PIN	FRAME LOC
CHASSIS GND		1	
SOLENOID GND		17	
TCHAN^0	♦	2	T20V
TCHAN^1	♦	18	T20W
MCHAN^0	♦	3	T21V
MCHAN^1	♦	19	T21W
TM RETURN		4	T21gnd$_L$
0 RETURN		20	T24gnd$_L$
DCHAN$^0_1$	♦	5	T25V
DCHAN$^1_1$	♦	21	T25W
DCHAN$^0_2$	♦	6	T24V
DCHAN$^1_2$	♦	22	T24W
DCHAN$^0_3$	♦	7	T23V
DCHAN$^1_3$	♦	23	T23W
BMOTN$^1_0$	♦	8	U25P
BMOTN$^1_1$	♦	24	U25V
BU^0	♦	9	U25Z
BU^1	♦	25	U25X
		10	
		26	
		11	
		27	
		12	
		28	
		13	
		29	
		14	
		30	
0V		15	
-18V		31	
-15V		16	
-15 SOLENOID		32	

FC (DA)

NAME		PIN	FRAME LOC
TN$_0$	♦	1	W18L
TN$_1$	♦	17	W18U
TN$_2$	♦	2	W15L
TN$_3$	♦	18	W15U
TN$_4$	♦	3	W12L
TN$_5$	♦	19	W12U
TN$_6$	♦	4	W9L
TN$_7$	♦	20	W9U
TN$_8$	♦	5	W6L
TN$_9$	♦	21	W6U
TN$_{10}$	♦	6	W3L
TN$_{11}$	♦	22	W3U
TNEL	♦	7	V23L
OPR10	♦	23	U17P
OPR11	♦	8	U17T
OPR12	♦	24	U17W
OPR13	♦	9	U17Z
OPR14	♦	25	U16N
OPR15	♦	10	U16L
OPR16	♦	26	U16P
OPR17	♦	11	U16T
XL7	♦	27	U23Y
XL10	♦	12	U22N
XL11	♦	28	U22K
XL12	♦	13	U22M
XL13	♦	29	U22P
INTERNAL CLOCK INHIBIT	◇	14	S9W
INTREQ	◆	30	#224
BDOINFF^1	◆	15	X19X
SAMFF^1	◆	32	V16H

RCD LINC ONLY

FD (DB)

NAME		PIN	FRAME LOC
UN$_0$	♦	1	X18L
UN$_1$	♦	17	X18U
UN$_2$	♦	2	X15L
UN$_3$	♦	18	X15U
UN$_4$	♦	3	X12L
UN$_5$	♦	19	X12U
UN$_6$	♦	4	X9L
UN$_7$	♦	20	X9U
UN$_8$	♦	5	X6L
UN$_9$	♦	21	X6U
UN$_{10}$	♦	6	X3L
UN$_{11}$	♦	22	X3U
UNEL	♦	7	V22L
CLEL	♦	23	V3F
BEGT	♦	1	U25H
MINP	♦	24	U25M
MOUT	♦	9	U25K
OPR0	♦	25	U18H
OPR1	♦	10	U18L
OPR2	♦	26	U18P
OPR3	♦	11	U18T
OPR4	♦	27	U18W
OPR5	♦	12	U18Z
OPR6	♦	28	U17H
OPR7	♦	13	U17L
XL0	♦	29	U24H
XL1	♦	14	U24K
XL2	♦	30	U24M
XL3	♦	15	U24P
XL4	♦	31	U23S
XL8	♦	16	U23U
XL6	♦	32	U23W

FE (DC)

NAME		PIN	FRAME LOC
GA$_0$	♦	1	W28Z
GA$_1$	♦	17	W25W
GA$_2$	♦	2	W25T
GA$_3$	♦	18	W25P
GA$_4$	♦	3	W25L
GA$_5$	♦	19	W25H
GA$_6$	♦	4	W24Z
GA$_7$	♦	20	W24W
GA$_8$	♦	5	W24T
GA$_9$	♦	21	W24P
GA$_{10}$	♦	6	W24L
GA$_{11}$	♦	22	W24H
ALEL	♦	7	U25P
AREL	♦	23	U25S
SN$_0$	♦	8	W18P
SN$_1$	♦	24	W18Y
SN$_2$	♦	9	W15P
SN$_3$	♦	25	W15Y
SN$_4$	♦	10	W12P
SN$_5$	♦	26	W12Y
SN$_6$	♦	11	W9P
SN$_7$	♦	27	W9Y
SN$_8$	♦	12	W6P
SN$_9$	♦	28	W6Y
SN$_{10}$	♦	13	W3P
SN$_{11}$	♦	29	W3Y
SNEL	♦	14	V22Z
		30	
mode 0		15	
mod 1		31	
mode 2		16	
mode 3		32	

FF (DD)

NAME		PIN	FRAME LOC
BB$_0$	♦	1	W22Z
BB$_4$	♦	18	W22X
BB$_2$	♦	2	W22V
BB$_3$	♦	18	W23Z
BB$_4$	♦	1	W23X
BB$_5$	♦	19	W23V
BB$_6$	♦	4	W23T
BB$_7$	♦	20	W23R
BB$_8$	♦	5	W23N
BB$_9$	♦	21	W23L
BB$_{10}$	♦	6	W23J
BB$_{11}$	♦	22	W23F
VN$_0$	♦	7	X18M
VN$_1$	♦	23	X18T
VN$_2$	♦	8	X15M
VN$_3$	♦	24	X15T
VN$_4$	♦	9	X12M
VN$_5$	♦	25	X12T
VN$_6$	♦	10	X9M
VN$_7$	♦	26	X9T
VN$_8$	♦	11	X6M
VN$_9$	♦	27	X6T
VN$_{10}$	♦	11	X3M
VN$_{11}$	♦	28	X3T
VNEL	♦	11	V22T
BR$_0$	♦	29	W22T
BR$_1$	♦	14	W22R
BR$_2$	♦	30	W22N
BR$_3$	♦	15	W22L
BR$_4$	♦	31	W22J
BR$_5$	♦	16	W22P

FH (DE)

NAME		PIN	FRAME LOC
CHASSIS		1	
0V		17	
ANCH17	◆	2	V17X
ANCH17	◇	18	V17gnd$_L$
		3	
		19	
		4	
0V±18 Return		20	V15SO
+18V		5	V17SO
-18V		21	V19SO
ANCN10	◆	6	V18H
ANCH10	◇	22	V18gnd$_U$
ANCN11	◆	7	V18M
ANCN11	◇	23	V18gnd$_U$
ANCN12	◆	8	V18T
ANCN12	◇	24	V18gnd$_L$
ANCN13	◆	9	V18X
ANCN13	◇	25	V18gnd$_L$
ANCH14	◆	10	V17N
ANCN14	◇	26	V17gnd$_U$
ANCN15	◆	11	V17M
ANCH15	◇	27	V17gnd$_U$
ANCN16	◆	12	V17T
ANCN16	◇	28	V17gnd$_L$
		13	
		29	
		14	
		30	
		15	
		31	
-15V		16	
		32	

FJ (DF)

NAME		PIN	FRAME LOC
CHASSIS		1	
0V		17	
		2	
		18	
		3	
		19	
		4	
		20	
		5	
		21	
QKRESTART	▶	6	V21N
QKRESTART	▷	22	V21D
BCPL	▶	7	V25J
BCPL	▷	23	V25H
BATPL	▶	8	V25S
BATPL	▷	24	V25T
BPRESET	▶	9	V25V
BPRESET	▷	25	V25X
BBEOP	▶	10	V24J
BBEOP	▷	26	V24H
BOPR·2.1	▶	11	V24S
BOPR·2.1	▷	27	V24T
BOPR·2.2	▶	12	V24V
BOPR·2.2	▷	28	V24X
EXT CLOCK	▶	13	M1E
EXT CLOCK	▷	29	M1D
+10V		14	
+10V		30	
		15	
		31	
-18V		16	
0V		32	

MAGNETIC TAPE CONNECTOR

TERMINAL FRAME CONNECTORS

Bold face is common on main type ( ) indicates connector at D.Term. Box

DATE		LINC	CHANGE LETTER	CHANGED BY	APP'D BY	DATE	CHANGES
ENGR							
1032		FANTAIL PIN ASSIGNMENTS SHEET #1					
CK							

L/T - 36 - 1033

FT (SCOPES)

NAME		PIN	FRAME LOC
CHASSIS		1	GD AT F.T.
		17	
VDEPLECTION		2	V13F
YRETURN		18	V13D
KDEPLECTION		3	V7F
XRETURN		19	V7D
		4	
		20	
OFPINT	►	5	V21V
OFPINT	▷	21	V21X
$KNOB^0$		6	V18E
$KRTN^0$		22	V19gnd
XNOB2		7	V18R
XRTN2		23	V19gnd
KNOB4		8	V17E
KRTN4		24	V16gnd
KNOB6		9	V17R
KRTN6		25	V16gnd
+6 VOLTS		10	V16P
-6 VOLTS		26	V16E
$ONINT_0$	►	11	V23P
$ONINT_0$	▷	27	V23R
$ONINT_1$	►	12	V23W
$ONINT_1$	▷	28	V23K
KNOB1		13	V18K
KRTN1		29	V19gnd
XNOB3		14	V18V
KRTN3		30	V19gnd
KNOB5		15	V17K
KRTN5		31	V16gnd
KNOB7		16	V17V
XRTN7		32	V16gnd

SCOPE CONNECTOR

FL (CA)

NAME		PIN	FRAME LOC
DV		1	
OV		17	
RS^1_8	◆	2	V14J
LS^0_5	◆	18	V24S
RS^1_9	◆	3	V14W
LS^1_5	◆	19	V24U
RS^1_{10}	◆	4	X3F
LS^0_6	◆	20	Y24M
RS^1_{11}	◆	5	K3V
LS^1_6	◆	21	V24P
LS^0_0	◆	6	V25W
LS^0_7	◆	22	Y24H
LS^1_0	◆	7	Y25V
LS^1_7	◆	23	Y24K
LS^0_1	◆	4	Y25S
LS^0_8	◆	25	Y23P
LS^1_1	◆	4	Y25U
LS^1_8	◆	25	Y23Y
LS^0_2	◆	10	Y25M
LS^0_9	◆	25	Y23S
LS^1_2	◆	13	Y25P
LS^1_9	◆	27	Y23U
LS^0_3	◆	12	Y25H
LS^0_{10}	◆	28	Y25U
LS^1_3	◆	13	Y25K
LS^1_{10}	◆	29	Y23P
LS^1_4	◆	14	V24W
RS^1_7	◆	30	Y15W
LS^1_4	◆	15	V24Y
LS^1_{11}	◆	31	V7W
-15V		16	
-15V		32	

FM (CB)

NAME		PIN	FRAME LOC
DV		1	
DV		17	
XOESTDPPB	◆	2	52U
ST400PB	◇	18	S13S
ISTOPFB	◆	3	S3U
ST20PB	◇	19	S13R
RESUMEPB	◇	4	S12W
STR5PB	◇	20	S13T
STEPPB	◇	5	S10H
IBIPB	◇	21	S11T
PBLC	◇	6	S8X
CBCPB	◇	22	S11U
DOPB	◇	7	S12V
PBLB	◇	23	S4U
PRESETFB	◇	8	S11S
RS^1_0	◆	24	V18J
PILLSTEPPB	◇	9	S12T
RS^1_1	◆	25	V18W
STEPEKPB	◇	10	S12U
RS^1_2	◆	26	Y17J
PBLA	◇	11	S1Y
RS^1_3	◆	27	Y17W
FILLPB	◇	12	S12R
RS^1_4	◆	28	Y16J
EXAMPB	◇	12	S12S
RS^1_4	◆	29	Y16W
MARKPB	◇	14	S13U
RS^1_6	◆	30	V15J
CLRPB	◇	15	S13V
AUTDFB	◆	31	R2U
-15V		16	
-15V		32	

FP (CC)

NAME		PIN	FRAME LOC
DV		1	
OV		17	
		2	
SS^1_5	◆	18	U23K
X RLSD	◇	3	X18W
		19	
KSTR	◇	4	U16V
		20	
XB^1_0	◆	5	X17P
		21	
KB^1_1	◆	6	K17Y
		22	
XB^1_2	◆	7	X14P
		23	
KB^1_3	◆	8	K14V
		24	
KB^1_4	◆	9	K11F
PBLD	◆	25	K19U
XB^1_5	◆	10	X11Y
RDLF	◇	26	K8J
SS^1_0	◆	21	U24S
RDLE	◇	27	K8H
SS^1_1	◆	21	U24U
RDLD	◇	28	K8F
SS^1_2	◆	13	U24W
RDLC	◇	29	K8E
SS^1_3	◆	14	U24V
RDLB	◇	30	K8X
SS^1_4	◆	15	U23N
RDLA	◇	31	K8Z
-15V		16	
-15V		32	

FN (CD)

NAME		PIN	FRAME LOC
OV		1	
OV		17	
S_0LT		2	V22Z
P_3LT		18	Y21T
S_1LT		3	Y22X
P_4LT		19	Y20Z
S_2LT		4	Y22V
P_5LT		20	Y20V
S_3LT		4	Y22T
P_6LT		21	Y20V
S_4LT		4	Y22R
P_7LT		22	Y20T
S_5LT		4	Y22N
P_8LT		21	Y20R
S_6LT		4	Y22L
P_9LT		24	Y20N
S_7LT		9	Y22J
C_6LT		28	Y19T
S_8LT		20	Y22F
C_7LT		26	Y19R
S_9LT		13	Y21R
C_8LT		27	Y19N
$S_{10}LT$		12	Y21N
P_9LT		28	Y19L
P_0LT		13	Y21Z
$C_{10}LT$		29	Y19J
P_1LT		14	Y21X
$C_{11}LT$		30	Y19L
P_2LT		15	V21V
AUDOUT		31	X17X
-15V		16	
-15V		32	

FR (CE)

NAME		PIN	FRAME LOC
OV		1	
OV		17	
R_0LT		2	W21T
EKAMLT		18	S14R
R_1LT		3	W21R
MARKLT		19	S14F
R_2LT		4	W21N
CLRLT		20	S14L
A_3LT		5	W21L
XOESTOPLT		21	S14T
A_3LT		4	W21J
ISTOPLT		22	S14X
R_5LT		7	W21F
AUTOLT		23	S14X
ECYLT		4	K17N
IBILT		25	S14T
ECYLT		4	K17L
CBCLT		25	S14T
XCYLT		10	K17J
C_0LT		25	Y20L
ICYLT		11	K17F
C_1LT		27	Y20J
PAUSELT		12	K17T
C_2LT		28	Y20F
RUNLT		13	K17R
C_2LT		29	Y19Z
		14	
C_4LT		30	V19K
PILLLT		15	S14N
C_5LT		31	Y19V
-15V		16	
-15V		32	

FS (CF)

NAME		PIN	FRAME LOC
SOLGND		1	
SOLGND		17	
CHASSIS		2	
A_1LT		18	W21X
B_0LT		3	Y21L
A_2LT		19	W21V
B_3LT		4	Y21J
A_3LT		20	W20Z
B_2LT		5	Y21F
A_4LT		21	W20X
B_3LT		6	X24Z
B_3LT		22	W20V
B_4LT		7	X24X
B_6LT		23	W20T
B_6LT		8	X24V
C_2LT		24	W20R
B_6LT		9	X24T
B_6LT		25	W20N
C_2LT		10	X24R
A_9LT		26	W20L
B_8LT		11	X24N
$A_{10}LT$		27	W20J
B_9LT		12	X24L
$A_{11}LT$		28	W20F
$B_{10}LT$		13	K24J
LINXLT		29	X17V
$B_{11}LT$		14	X24P
RCHIME	◆	30	R13Z
A_0LT		15	W21Z
$RELIP^0$	◇	31	U16U
-15VSOL		16	
-15VSOL		32	

CONSOLE CONNECTORS

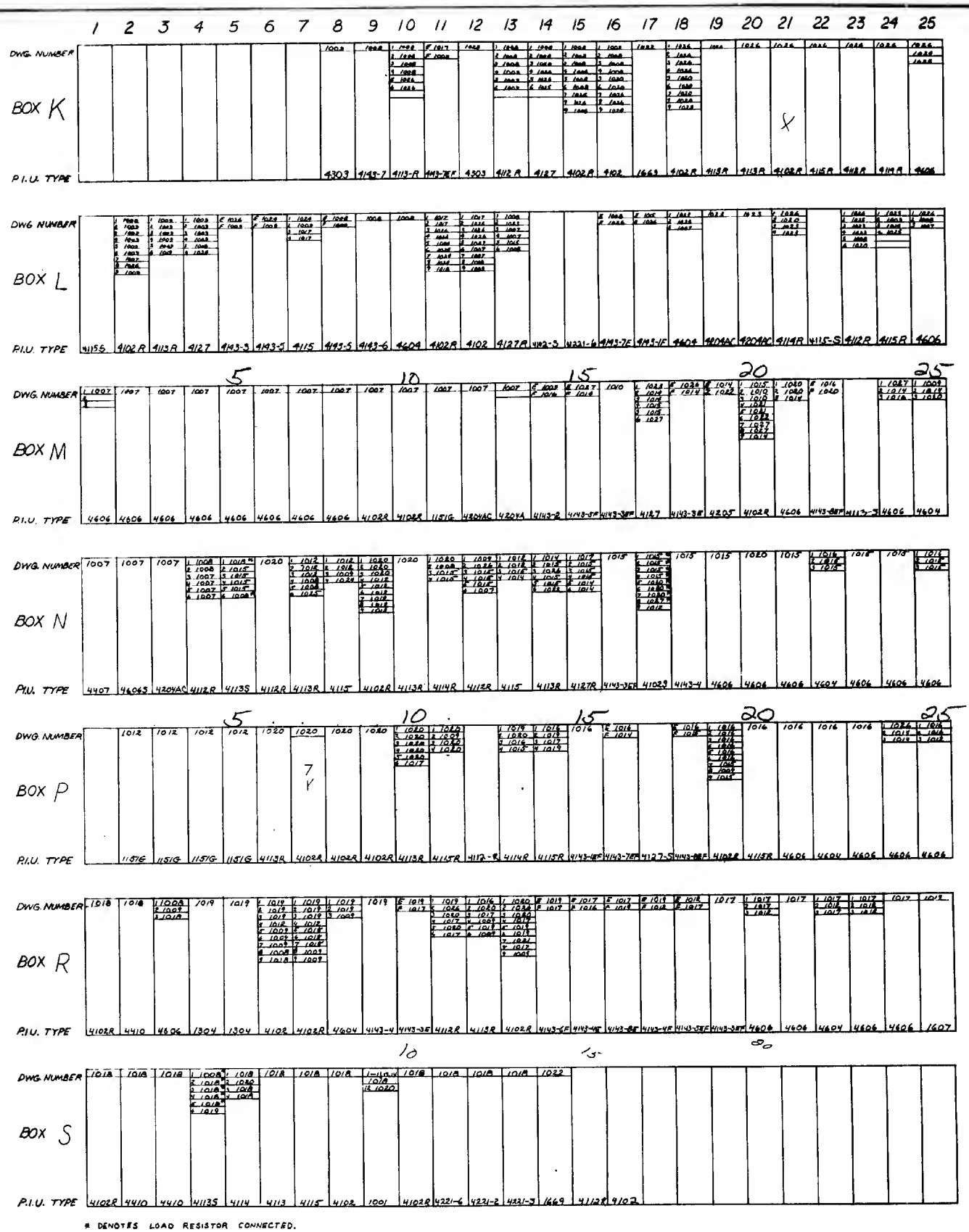
CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC

FANTAIL PIN ASSIGNMENTS SHEET #2

1033

DATE | ENG. | CK.



L/T - 37 - 1034

DATE			
1034	LINC	P.I.U. DRAWING NUMBER REFERENCE (CONTROL SIDE)	
CK			

L/T - 38 - 1035

BOX T

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1023	1023	1025	1023	1024 1025	1 1025 2 1024 3 1024	1 1025 2 1025 3 1025 4 1025 5 1024 6 1024 7 1024 8 9	1024	1024	1024	1024	1024	1024	1024	1024	1024	1 1024 2 1024 3 1024 4 1024 5 1021 6 1023			1023	1024		1024	1024	1024
P.I.U. TYPE	4303	4303	4303	4604	4205	4606S	4102	4115R	4112R	1151G	4205	4205	4127R	4127R	4205	4205	4113R			EP107	EP107		EP107	EP107	EP107

BOX U

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1023	1 1025* 2 1019 3 1024 4 1023 5 1023 6 1023	1025	1 1025 2 1025 3 1014 4 1024 5 1024 6 1023	1025	1 1014 2 1014 3 1014 4 1025 5 1024 6 1024 7 1024 8 1025 9 1018									1 1023 2 1020* 3 1020* 4 1025	1 1022 2 1022 3 1022 4 1022 5 1021 6 1020	1022	1022	1 1012 2 1012 3 1012 4 1012 5 1012 6 1012 7 1012 8 1012 9 1021	1012	1021	1021	1021	1021	1 1022 2 1020 3 1020 4 1020 5 1022 6 1022 7 1022 8 1022 9 1022
P.I.U. TYPE	4606	4127R	4205	4112R	4115R	4103R									4115S	4112R	4112R	4113R	4102R	4102R	4143-1	4143-1	4143-1EF	4143-1EF	4102R

BOX V

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1 1025 2 1014 3 1014	1 1025 2 1025 3 1025 4 1025 5 1025 6 1014	1 1020 2 1023 3 1025 4 1026	1014	1014	1010	1027	1027	1027	1027	1027	1027	1027	1027	1027	1027	1027	1027	1012	1012	1 1027 2 1009 3 1022	1 1016 2 1016 3 1015	1 1015 2 1022 3 1022	1022	1022
P.I.U. TYPE	4604	4127	4114R	4221-4	4221-5	4127	1561	4677	4677	4677	4677	4677	1561	1561	EP108	EP103	EP104	EP104	1151E	1151G	4604	4606	4606	4604	4604

BOX W

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1021	1022	1022	1022	1022	1022	1022
P.I.U. TYPE	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4143-2EF	1669	1669	4102R	4102R	4113R	4112R

BOX X

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1 1013* 2 1011 3 1011 4 1010 5 1012 6 1012 7 1012* 8 9	1 1014 2 1010 3 1010 4 1010 5 1010 6 1010	1 1010 2 1021 3 1021 4 1021 5 1013 6 1013	1019	1021	1022	1021
P.I.U. TYPE	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4102S	4127	4113R	4221-6	4143-2EF	1669	4143-2EF

BOX Y

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1028	1028	1028	1028	1028	1028	1012	1012	1012	1012	1012	1012	1 1012* 2 1013 3 1012* 4 1011 5 1013* 6 1013*	1013	1013	1013	1013	1013	1022	1022	1022	1022	1021	1021	1021
P.I.U. TYPE	1571	1571	1571	1571	1571	1571	4204A	4204A	4204A	4204A	4204AC	4204AC	4127S	4204AC	4204AC	4204AC	4204AC	4204AC	1669	1669	1669	1669	4143-1	4143-1	4143-1EF

BOX Z

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER											1030	1030	1030	1030	1030	1030		1029	1029	1013	1013	1013	1013	1013	1013
	← MEMORY (columns 1–10) →																								
P.I.U. TYPE											EP102	EP102	EP105	EP105	EP105	EP105		EP101	EP101	4204AC	4204AC	4204AC	4204AC	4204AC	4204AC

* DENOTES LOAD RESISTOR CONNECTED.

1. E	10 R
2. F	11 S
3. H	12. T
4. J	13. U
5. K	14. V
6. L	15. W
7. M	16. X
8. N	17. Y
9. P	18. Z

1001

1. E,F
2. H,J
3. K,L
4. M,N
5. P,R
6. S,T
7. U,V
8. W,X
9. Y,Z

4102

1. E,F,H
2. J,K,L
3. M,N,P
4. R,S,T
5. U,V,W
6. X,Y,Z

4112 + 4113

1. E,F,H,J,K
2. L,M,N,P,R
3. S,T,U,V
4. W,X,Y,Z

4114 + 4115

1. E,F,H
2. J,K,L
3. M,N,P
4. R,S,T
5. U,V,W
6. X,Y,Z

1. E,F,H,J,K,L,M,N,P
2. R,S,T,U,V,W,X,Y,Z

4205

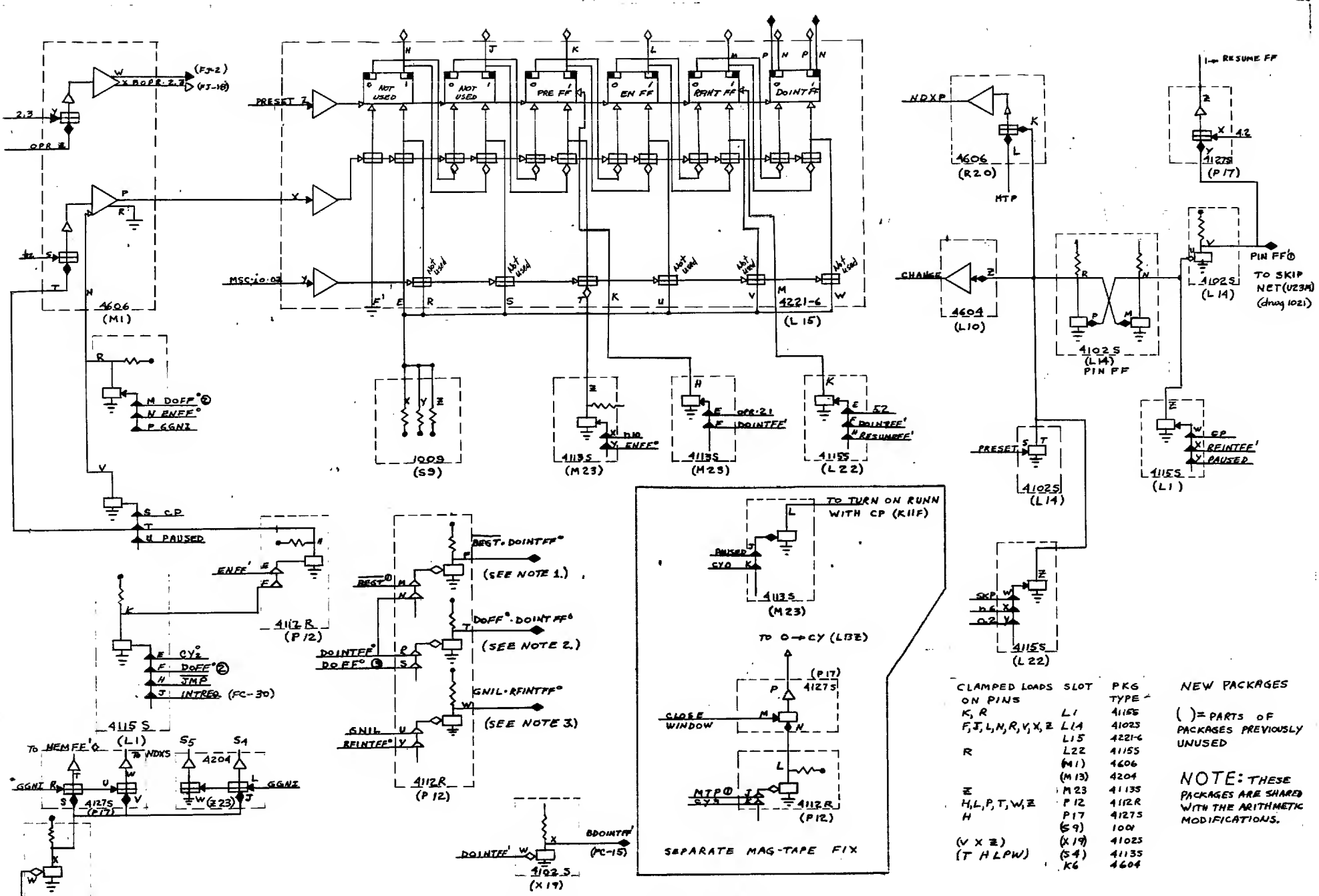
1. E,F,H,J,K,L
2. M,N,P,R,S,T
3. U,V,W,X,Y,Z

4604 + 4606

LINC

P.I.U. DRAWING NUMBER REFERENCE (REGISTER SIDE)

1035



CLAMPED LOADS ON PINS	SLOT	PKG TYPE
K, R	L1	4115S
F, J, L, N, R, Y, X, Z	L14	4102S
	L15	4221-6
R	L22	4115S
	(M1)	4606
	(M13)	4204
Z	M23	4113S
H, L, P, T, W, Z	P12	4112R
H	P17	4127S
	(S9)	1009
(V X Z)	(X19)	4102S
(T H LPW)	(S4)	4113S
	K6	4604

NEW PACKAGES

( ) = PARTS OF PACKAGES PREVIOUSLY UNUSED

NOTE: THESE PACKAGES ARE SHARED WITH THE ARITHMETIC MODIFICATIONS.

NOTE 1. Replaces $\overline{\text{BEGT}}$◆(L17Z) in input logic to LBCOL (dwg 1015)

2. Replaces DOFF◆(R14L) in input logic to NDXP (dwg 1017)

3. Replaces GNIL◆(R24L) in input logic to P→S (dwg 1017)

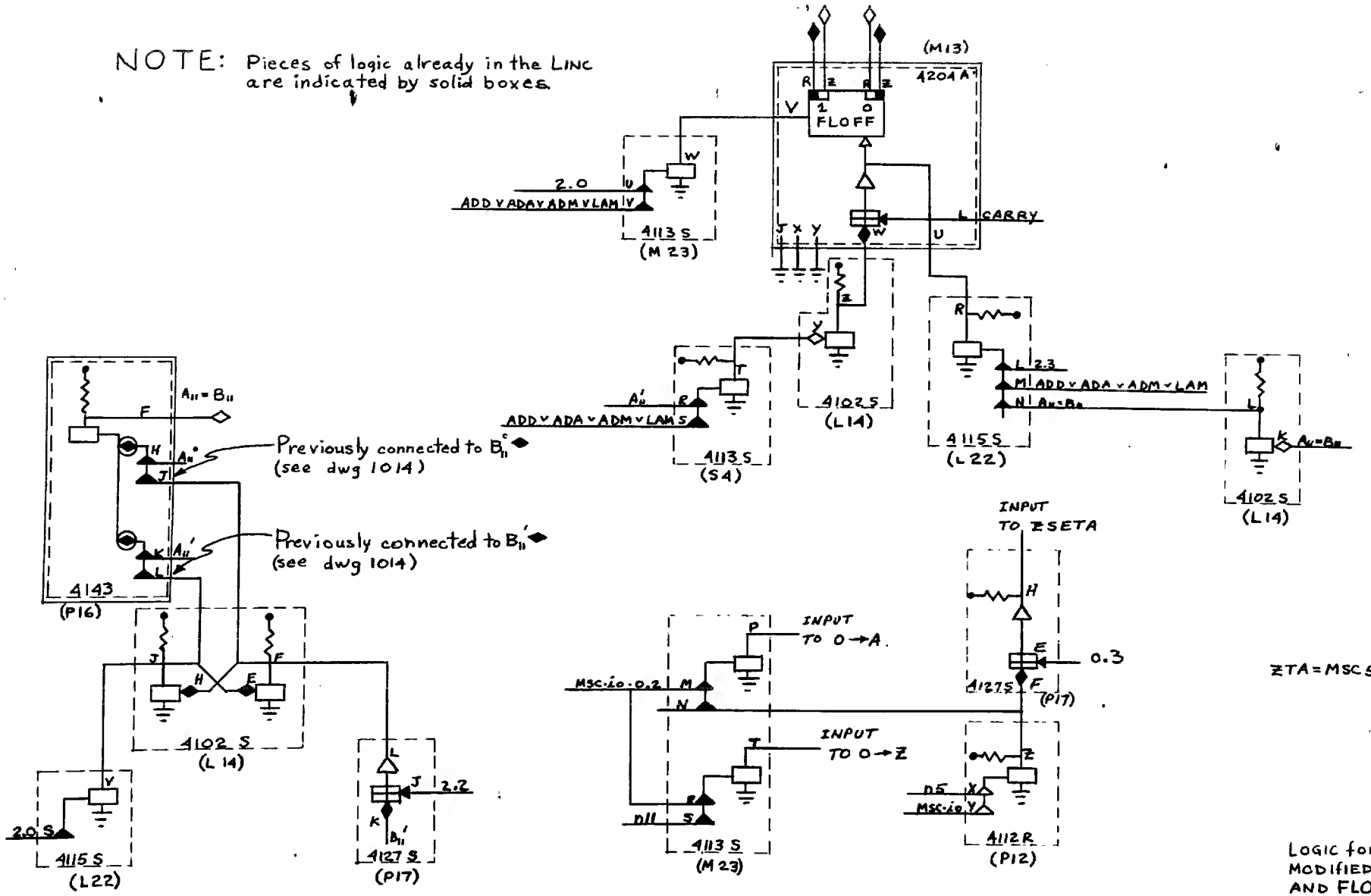
4. Preset (L6X) is replaced by 4.2 in the 0→WGFF Logic (dwg 1024) (MASTER RESET NOW PRODUCES 4.2)

LINC

Interrupt Logic and Additional MTP Logic

1090

NOTE: Pieces of logic already in the LINC are indicated by solid boxes.



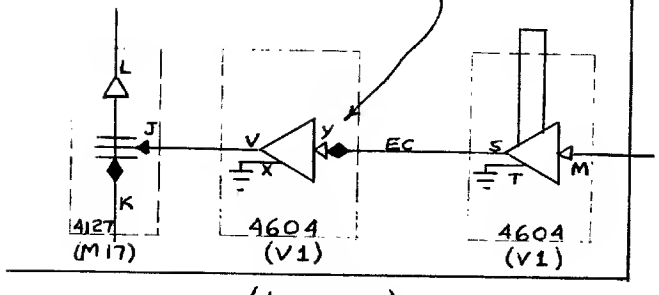
ZTA = MSC 5

LOGIC for ZTA, MODIFIED CLR, AND FLOFF.

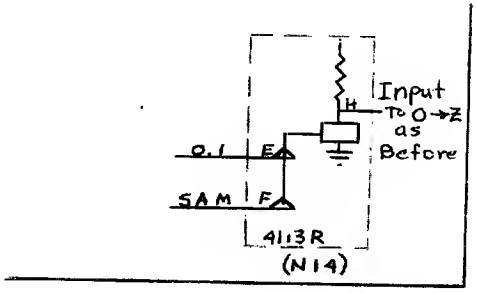
1091

TRIGGERS ON TRAILING EDGE
of NEGATIVE 1μsec PULSE

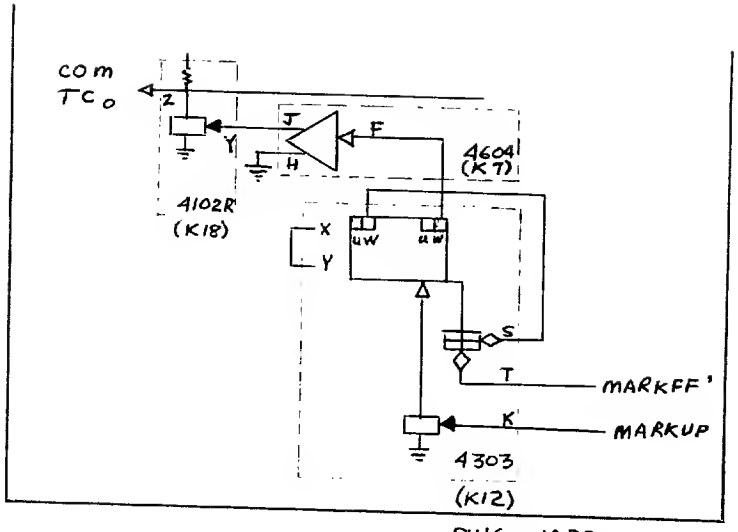
EC is now output of V1S, not V1V



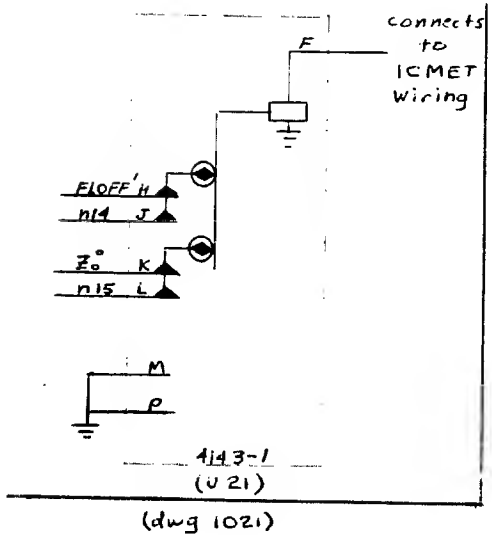
(dwg 1014)



(dwg 1014)



DWG 1023



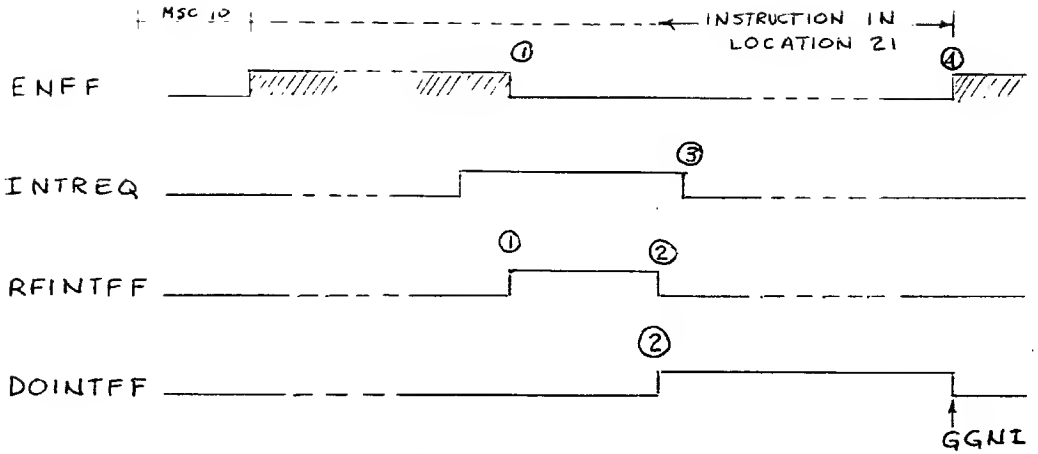
(dwg 1021)

FLO = SKP 14
ZZZ = SKP 15

PACKAGE
RE-ASSIGNMENTS FOR
NEW ARITHMETIC
INSTRUCTIONS

1092

ENI



INTERRUPT TIMING

① $t_2 \cdot$ INTREQ $\cdot \overline{\text{JMP}} \cdot$ ENFF$' \supset 1 \rightarrow$ RFINTFF, $0 \rightarrow$ ENFF

② GGNI $\cdot$ RFINTFF$' \supset 1 \rightarrow$ DOINTFF, $0 \rightarrow$ RFINTFF, INHIBIT P$\rightarrow$S, 21$\rightarrow$S

③ INTREQ Should be removed by BCPL $\cdot$ BDOINTFF$'$

④ Iff instruction in Loc 21 is OPR, $1 \rightarrow$ ENFF

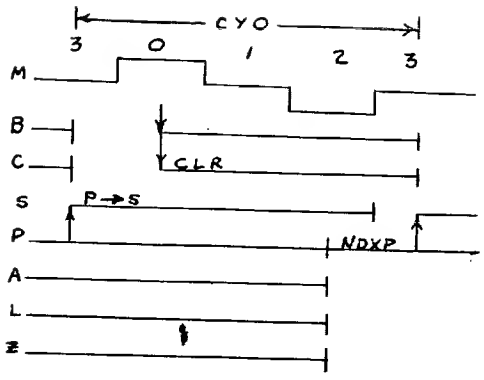
COMMENTS ON INSTRUCTION IN LOC 21 WHEN DOINTFF$'$

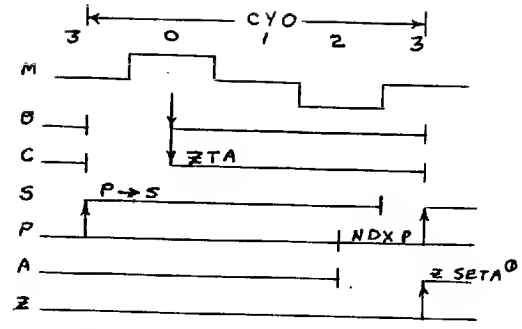
1. NDXP is inhibited

   This means that:
   - @ JMP will leave JMP P* in LOC 0.
   - ⓑ OPR will not affect P. Thus P$\rightarrow$S at end of OPR will return immediately to the next instruction of the main program.

2. BCOMA is inhibited during OPR. This means that Accumulator is undisturbed unless willfully affected by asserting SNEL, TNEL, or CLEL.

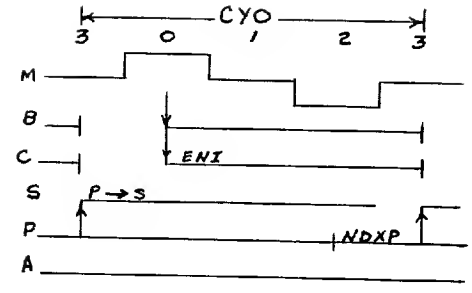
*P is address of next instruction in main program.





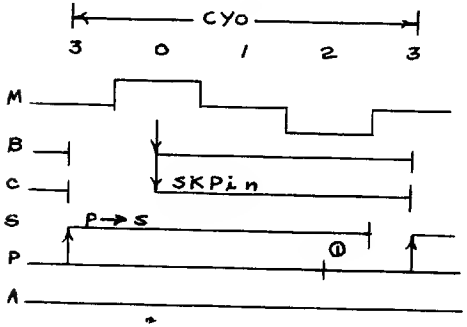
① ZSETA ⇒ $Z_i \rightarrow A_{i-1}$

ZTA = MSC 5



NOTE: 1 → PREFF at 0.2

ENI = MSC 10



① NDXP iff $\overline{\text{CMET}}$
2 NDXP iff CMET

New Skip Instruction

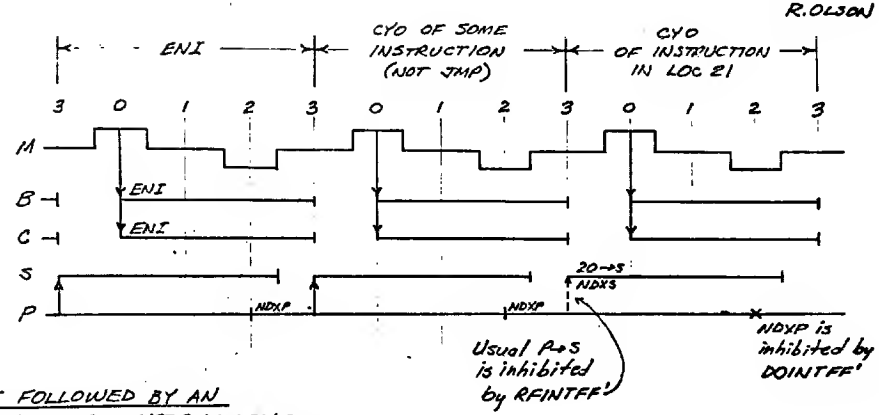
SIN (SKP6) "Skip iff PINFF'
FLO (SKP14) Skip iff FLOFF'
ZZZ (SKP15) Skip iff Z_0^0

Note: SIN also clears PINFF

New Instruction
and
Modified CLR
1094

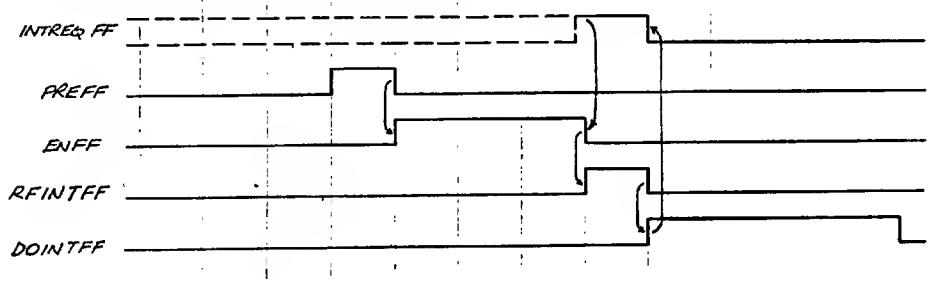
ENI & DIN TIMING DIAGRAM

10-27-71
R.OLSON



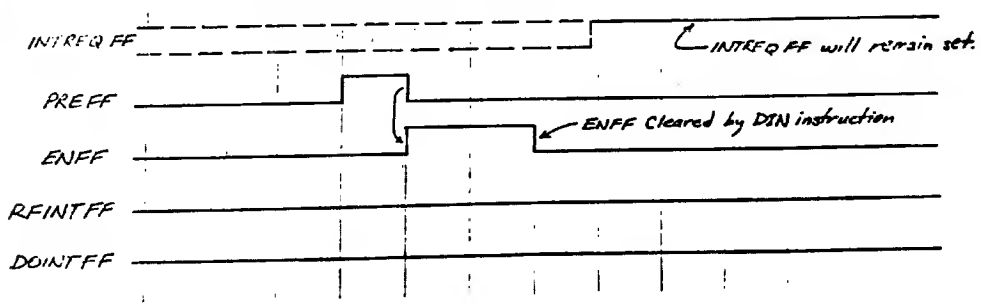
ENI FOLLOWED BY AN INTERRUPTED INSTRUCTION:

(Not necessarily immediately following ENI)



ENI FOLLOWED BY DIN INSTRUCTION:

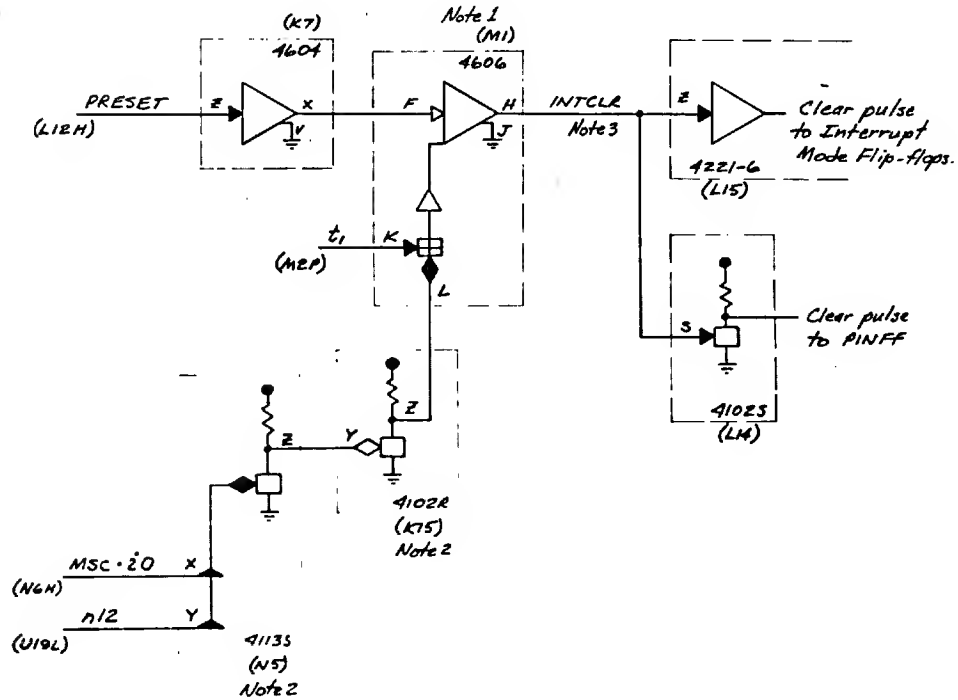
(Also not necessarily immediately following ENI)



DISABLE INTERRUPT (DIN) MODIFICATION

CLASSIC LINC

10-27-71
R.OLSON



Notes:
1. Formerly used for Ext Clock, refer to Linc Drwg. 1007
2. These gates were no longer used following a 1966 modification, refer to Linc Drwg. 1008. (true of LCF Lincs also.)
3. PRESET used to connect to L15Z and L14S.